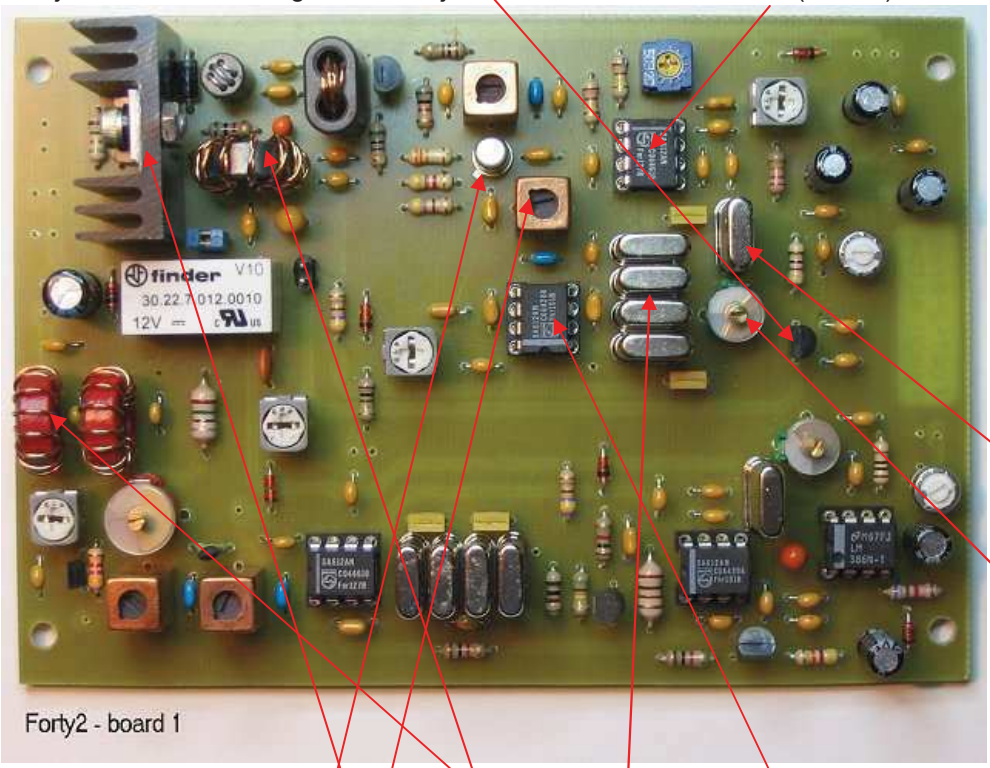
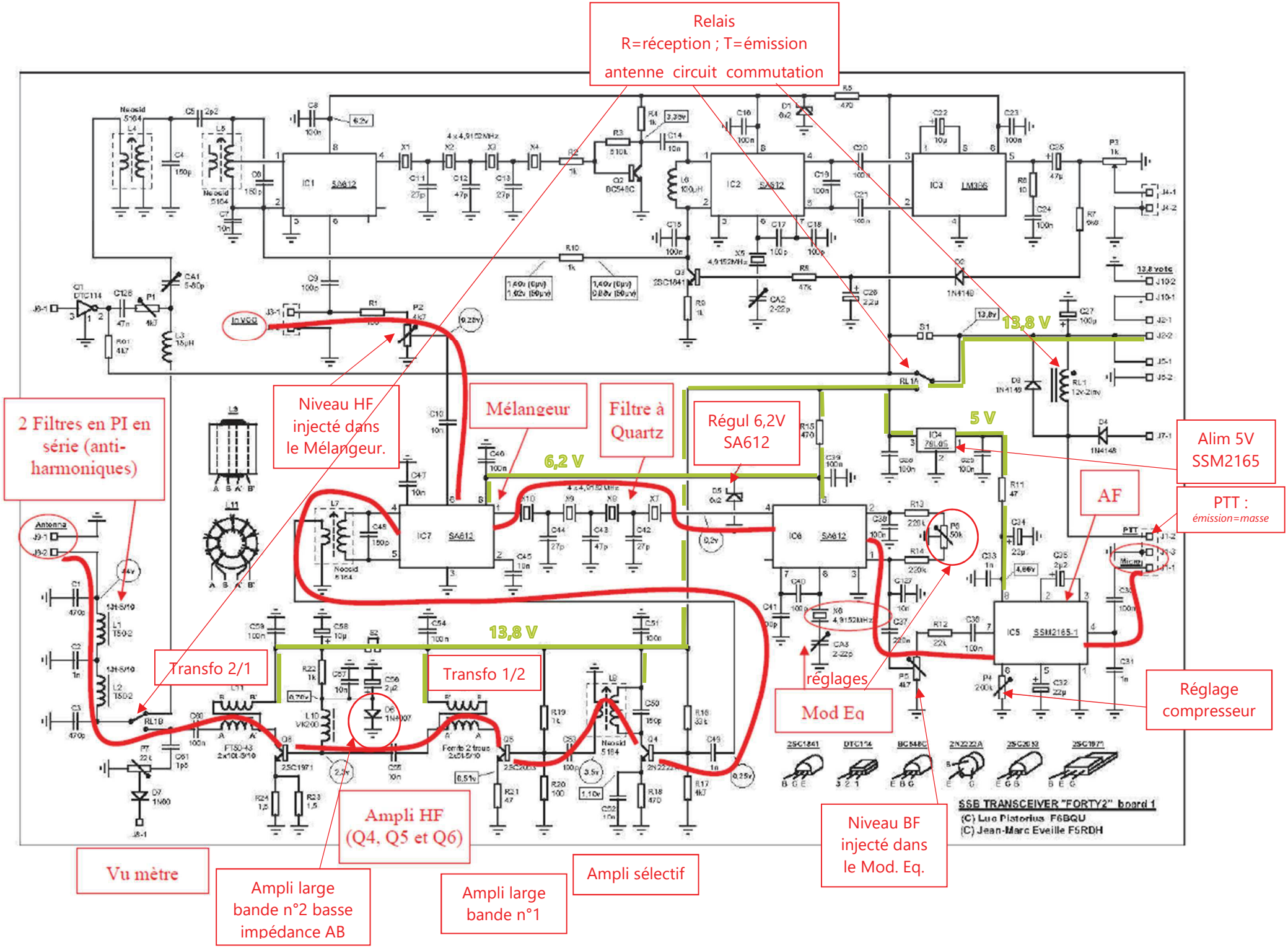
<u>Détails émetteur</u> (schéma " board 1 ") :
Le signal issu du microphone (de préférence un modèle dynamique basse impédance) est appliqué à l'entrée 4 de IC5. Le condensateur de découplage C31 est utile lors de l'utilisation d'un microphone haute impédance, et contre les retours HF. Le SSM2165-1 est un préamplificateur BF faible bruit, incorporant un compresseur de modulation et un réducteur de bruit ambiant. Le taux de compression est ajustable avec un rapport de 1/1 (sans compression) à 15/1. Le réglage se fait par variation de la résistance sur la broche 6 du circuit. 0 ohm correspond à un rapport de 1/1 et 250 Kohms à un rapport de 15/1. Sur notre circuit se trouve une résistance ajustable de 200 Kohms (P4). On peut donc faire varier le taux de 1/1 à 1/12. Mais il est inutile de dépasser 1/8, suffisamment efficace sans aucune distorsion. Le circuit fonctionnant exclusivement sous 5 volts, il a été ajouté un régulateur de tension (IC4).

P5 ajuste le niveau du signal avant injection sur la broche 1 de IC6 (SA612). C127 évite le déréglage du modulateur équilibré en fonction de la position de P5. IC6 est monté en modulateur équilibré, avec gain, générant le signal HF en DSB (double bande latérale avec réduction de porteuse) sur la broche 4. La fréquence de ce signal est déterminée par le quartz X6 de 4,9152 MHz. CA3 permet d'ajuster finement la fréquence du signal d'émission par rapport à celle de réception. P6 permet d'ajuster au maximum de réjection de porteuse. La bande latérale indésirable est supprimée par le filtre à 4 quartz faisant suite à IC6. Le signal du VCO (issu du synthétiseur), dont le niveau est ajusté par P2, est mélangé dans IC7 (SA612) au signal BLU issu du filtre à quartz. Seule la fréquence utile dans la bande des 40m est filtrée en sorties 4 et 5 de IC7 par le circuit résonant parallèle L7-C48. La tension d'alimentation des circuits IC6 et IC7 est fixée à 6,2 volts par la diode zener D5. Les trois étages d'amplification amènent le signal utile à une puissance de près de 5 watts HF. L'étage Q4 est un amplificateur sélectif, alors que les deux étages suivants sont à large bande. Le transistor de puissance Q6 ayant entrée et sortie à très basse impédance, l'utilisation de transformateurs abaisseur (L9) et élévateur (L11) d'impédance a été adoptée pour un transfert d'énergie maximum. La diode D6 et la résistance R22 fixent, au travers de la self d'isolement HF L10, la tension de polarisation de base du transistor Q6 à 0,7 volts pour un fonctionnement de cet étage en classe AB linéaire. Une partie infime de la HF est prélevée (C61, P7) et redressée (D7) pour l'indicateur de puissance. La sortie vers l'antenne se fait au travers du filtre passe-bas C3-L2-C2-L1-C1, afin de rejeter au maximum les harmoniques indésirables




Relais
R=réception ; T=émission
antenne circuit commutation
2 Filtres en PI en série (anti-harmoniques)
Niveau HF injecté dans le Mélangeur.
Mélangeur
Filtre à Quartz
Régul 6,2V SA612
Alim 5V SSM2165
AF
PTT :
émission=masse
Transfo 2/1
Transfo 1/2
Ampli HF (Q4, Q5 et Q6)
Vu mètre
Ampli large bande n°2 basse impédance AB
Ampli large bande n°1
Ampli sélectif
Niveau BF injecté dans le Mod. Eq.
Mod Eq
réglages
Réglage compresseur
13,8 V
6,2 V
5 V
SSB TRANSCEIVER "FORTY2" board 1
(C) Luc Pistorius F6BQU
(C) Jean-Marc Eveille F5RDH

SA612A

Double-balanced mixer and oscillator

Rev. 3 — 4 June 2014 Product data sheet

1. General description

The SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low-power communication systems with signal frequencies to 500 MHz and local oscillator frequencies as high as 200 MHz. The mixer is a 'Gilbert cell' multiplier configuration that provides gain of 14 dB or more at 45 MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external LO. Noise figure at 45 MHz is typically below 6 dB and makes the device well-suited for high-performance cordless phone/cellular radio. The low power consumption makes the SA612A excellent for battery-operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The SA612A is available in an 8-lead SO (surface-mounted miniature package).

2. Features and benefits

- Low current consumption
- Low cost
- Operation to 500 MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

3. Applications

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonobuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SA612AD/01	SA612A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SA612AD/01	SA612AD/01,112	SO8	Standard marking *IC's tube - DSC bulk pack	2000	T_{amb} = −40 °C to +85 °C
	SA612AD/01,118	SO8	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

5. Block diagram

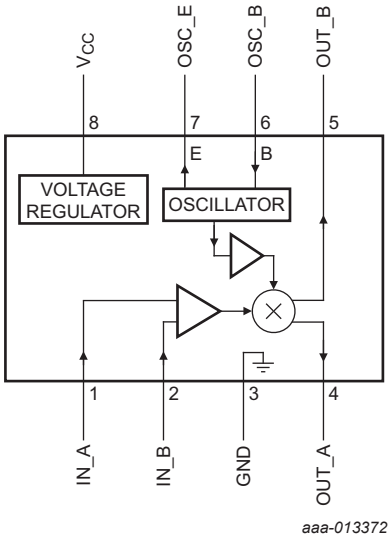


Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

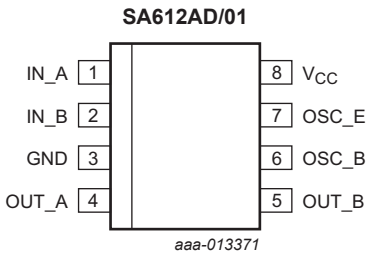

Fig 2. Pin configuration for SO8

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
IN_A	1	RF input A
IN_B	2	RF input B
GND	3	ground
OUT_A	4	mixer output A
OUT_B	5	mixer output B
OSC_B	6	oscillator input (base)
OSC_E	7	oscillator output (emitter)
V_{CC}	8	supply voltage

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7. Functional description

The SA612A is a Gilbert cell, an oscillator/buffer, and a temperature-compensated bias network as shown in Figure 3. The Gilbert cell is a differential amplifier (IN_A and IN_B pins) that drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

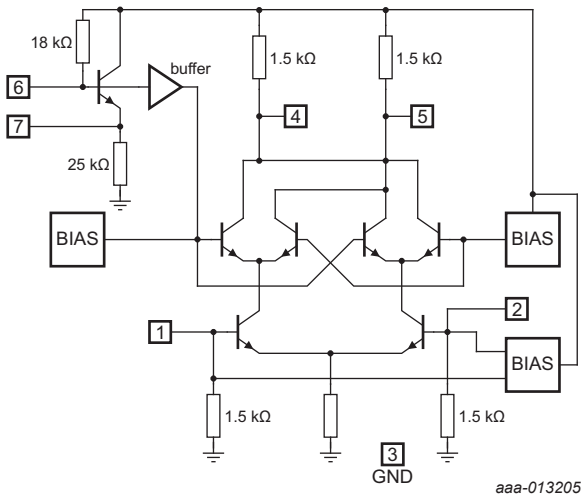

Fig 3. Equivalent circuit

The SA612A is designed for optimum low-power performance. When used with the SA614A as a 45 MHz cordless phone/cellular radio second IF and demodulator, the SA612A is capable of receiving −119 dBm signals with a 12 dB S/N ratio. Third-order intercept is typically −15 dBm (that is approximately +5 dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the SA612A should be appropriately scaled.

Besides excellent low-power performance well into VHF, the SA612A is flexible. The input, output and oscillator ports support various configurations provided the designer understands certain constraints, which are explained here.

The RF inputs (IN_A and IN_B pins) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5 kΩ || 3 pF through 50 MHz. IN_A and IN_B pins can be used interchangeably, but they should not be DC biased externally. Figure 4 shows three typical input configurations.

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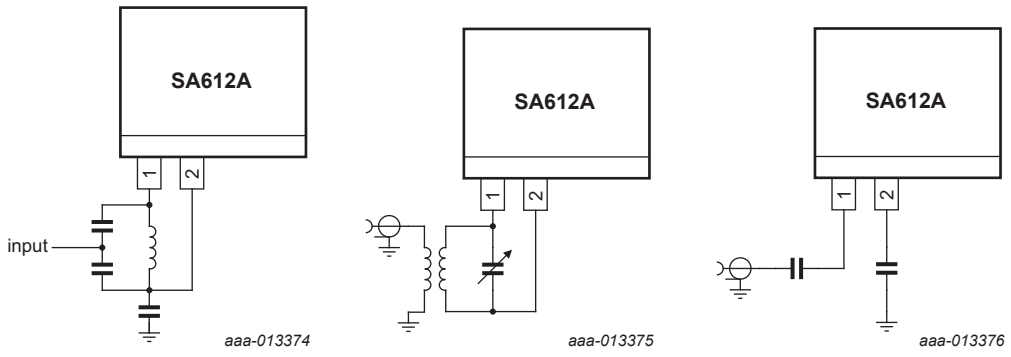


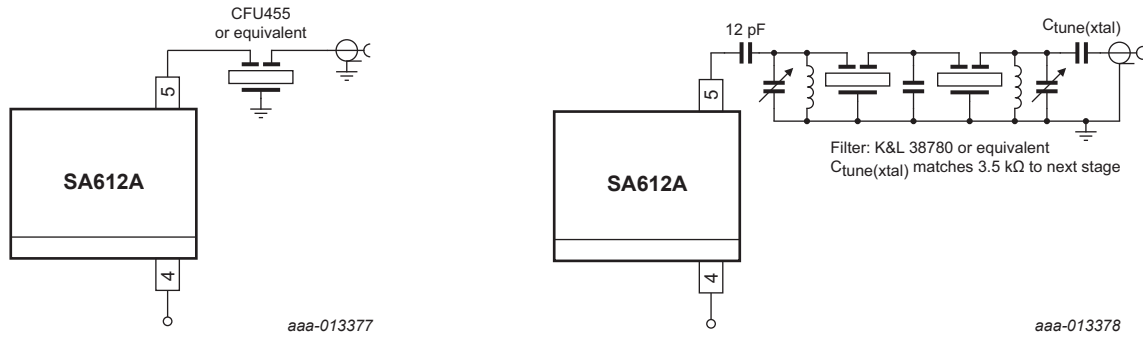
a. Single-ended tuned input

b. Balanced input (for attenuation of second-order products)

c. Single-ended untuned input

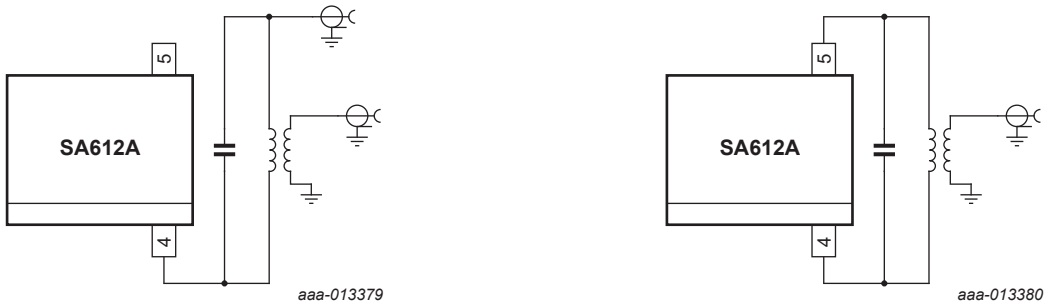
Fig 4. Input configuration

The mixer outputs (OUT_A and OUT_B pins) are also internally biased. Each output is connected to the internal positive supply by a 1.5 kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 5 shows three single-ended output configurations and a balanced output.



a. Single-ended ceramic filter

b. Single-ended crystal filter



c. Single-ended IFT

d. Balanced output

Fig 5. Output configuration

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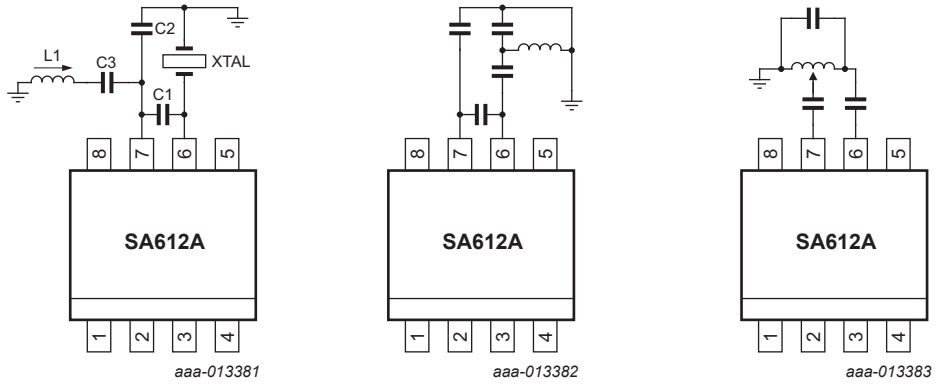
The oscillator can sustain oscillation beyond 200 MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank ‘Q’ and required drive levels. The higher the ‘Q’ of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at OSC_B (pin 6) through a DC blocking capacitor. External LO should be 200 mV (peak-to-peak) minimum up to 300 mV (peak-to-peak) maximum.

Figure 6 shows several proven oscillator circuits. Figure 6a is appropriate for cordless phones or cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation, the trap is omitted.



a. Colpitts crystal oscillator (overtone mode)

b. Colpitts L/C tank oscillator

c. Hartley L/C tank oscillator

Fig 6. Oscillator circuits

Figure 7 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal that assures correct system operation.

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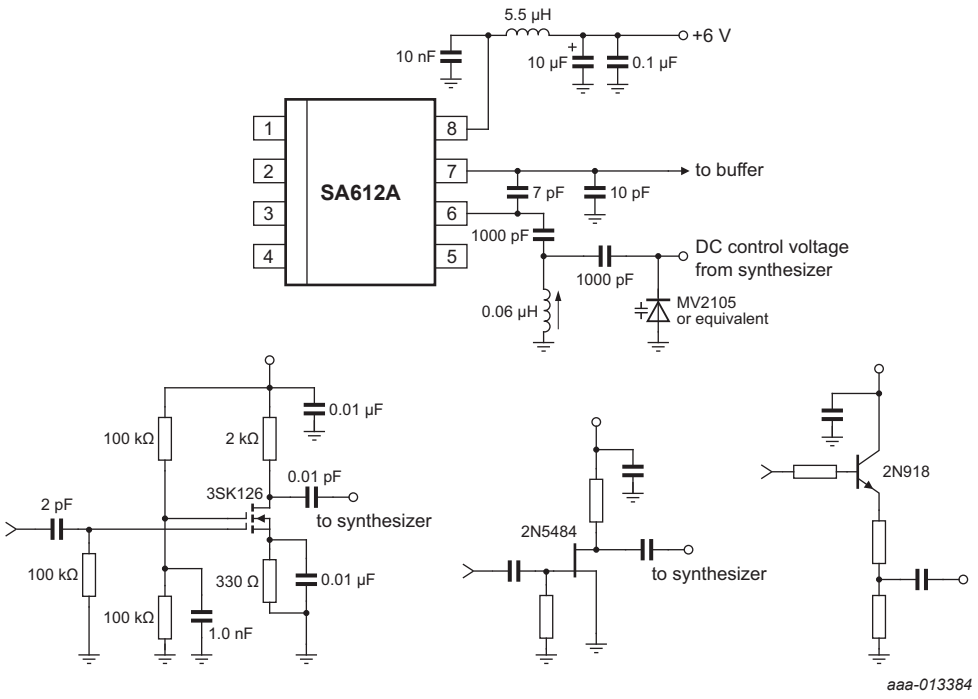

Fig 7. Colpitts oscillator suitable for synthesizer applications and typical buffers

8. Application design-in information

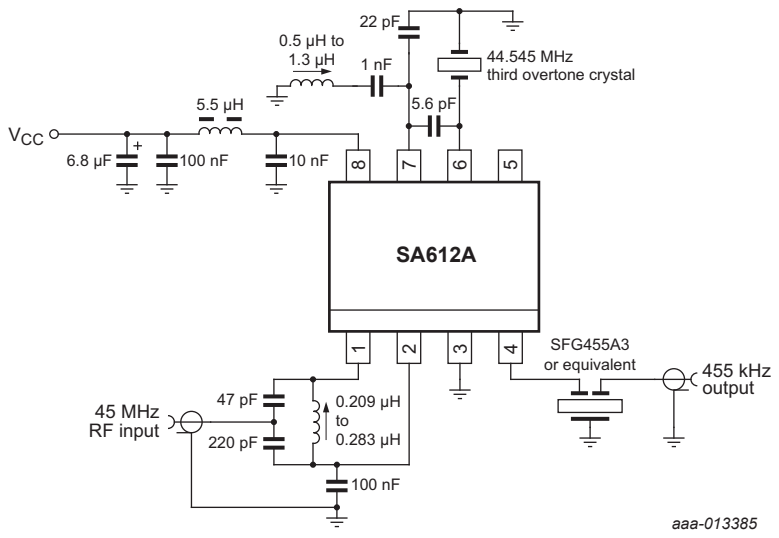

Fig 8. Typical application for cordless/cellular radio

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9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	9	V
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

10. Static characteristics

Table 5. Static characteristics

T_{amb} = 25 °C; V_{CC} = +6 V; unless specified otherwise. Refer to Figure 15.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	8.0	V
I_{CC}	supply current		-	2.4	3.0	mA

11. Dynamic characteristics

Table 6. Dynamic characteristics

T_{amb} = 25 °C; V_{CC} = +6 V; unless specified otherwise. Refer to Figure 15.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_i	input frequency		-	500	-	MHz
f_{osc}	oscillator frequency		-	200	-	MHz
NF	noise figure	at 45 MHz	-	5.0	-	dB
$IP3_i$	input third-order intercept point	RF input = –45 dBm; RF1 = 45.0 MHz; RF2 = 45.06 MHz	-	–13	-	dBm
G_{conv}	conversion gain	at 45 MHz	14	17	-	dB
$R_{i(RF)}$	RF input resistance		1.5	-	-	kΩ
$C_{i(RF)}$	RF input capacitance		-	3	-	pF
$R_{o(mix)}$	mixer output resistance	OUT_A, OUT_B pins	-	1.5	-	kΩ

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12. Performance curves

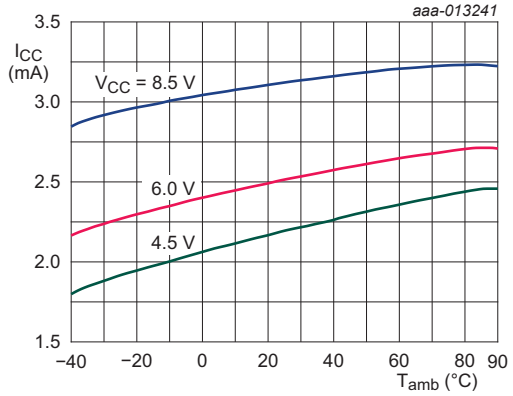


Fig 9. Supply current versus temperature

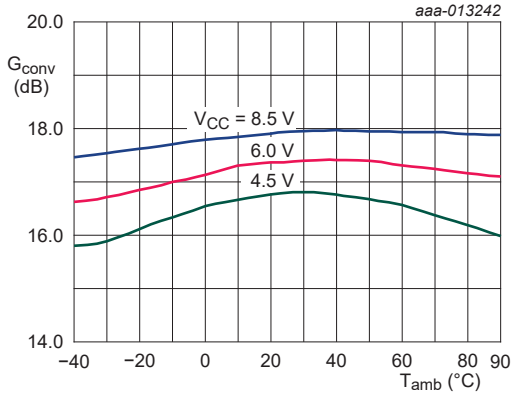


Fig 10. Conversion gain versus temperature

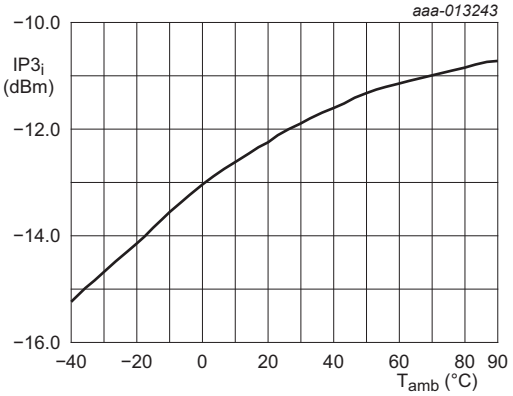


Fig 11. Third-order intercept point versus temperature

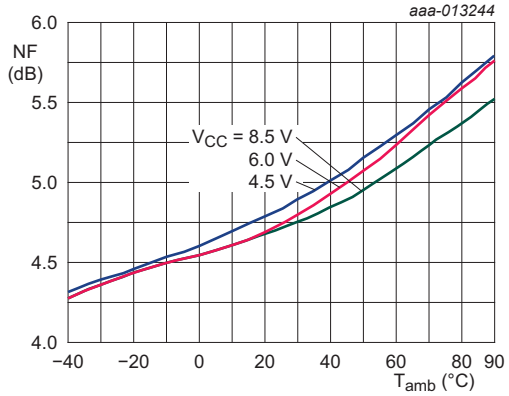
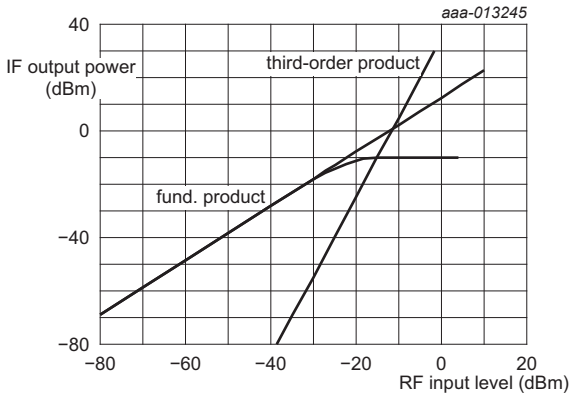


Fig 12. Noise Figure versus temperature



RF1 = 45 MHz; IF = 455 kHz; RF2 = 45.06 MHz

Fig 13. Third-order intercept and compression

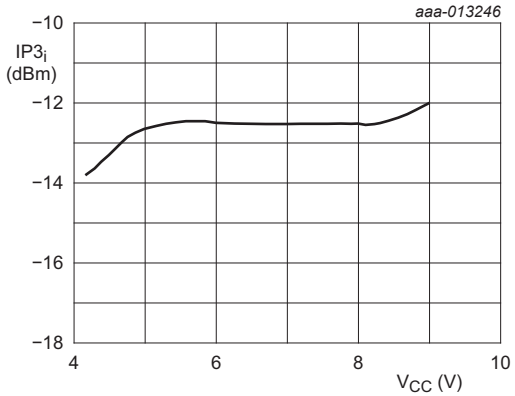


Fig 14. Input third-order intercept point versus supply voltage

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13. Test information

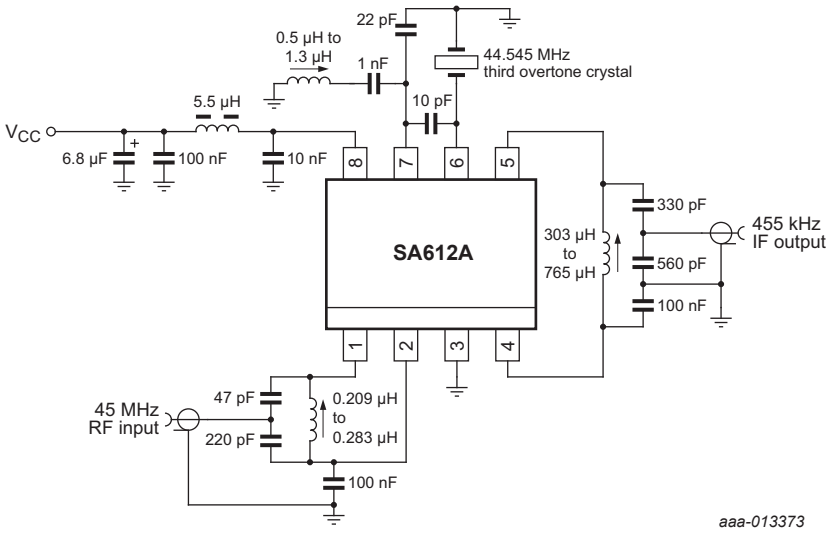

Fig 15. Test configuration

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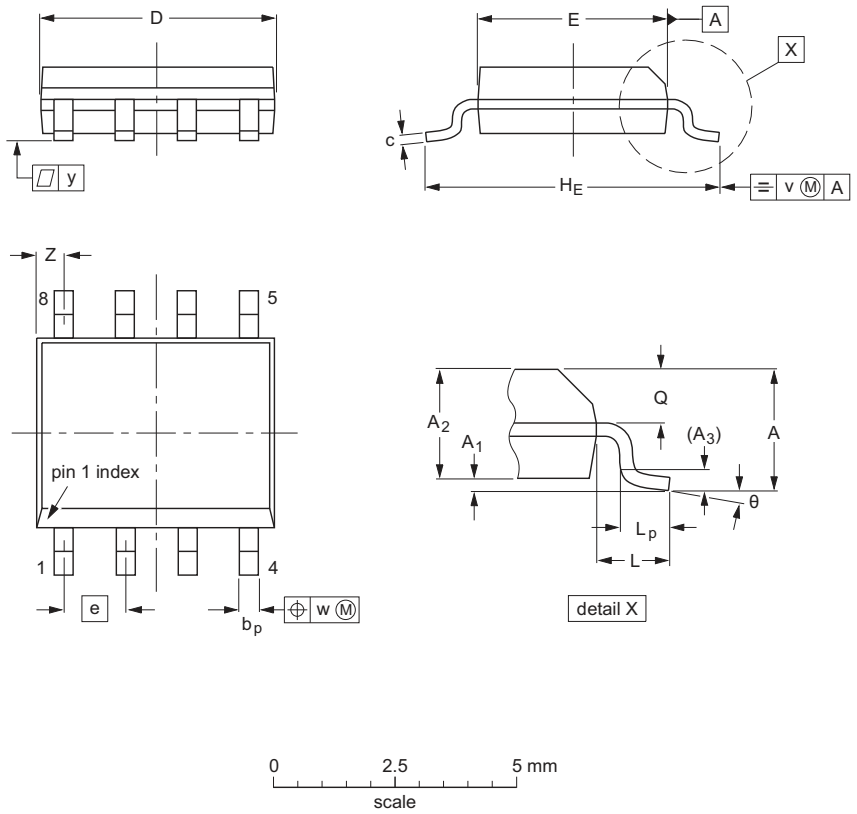
14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

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15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.

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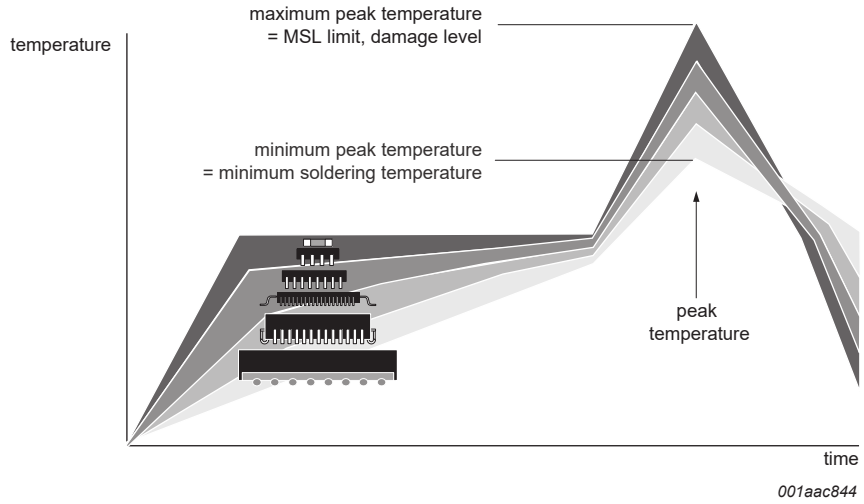

MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Soldering: PCB footprints

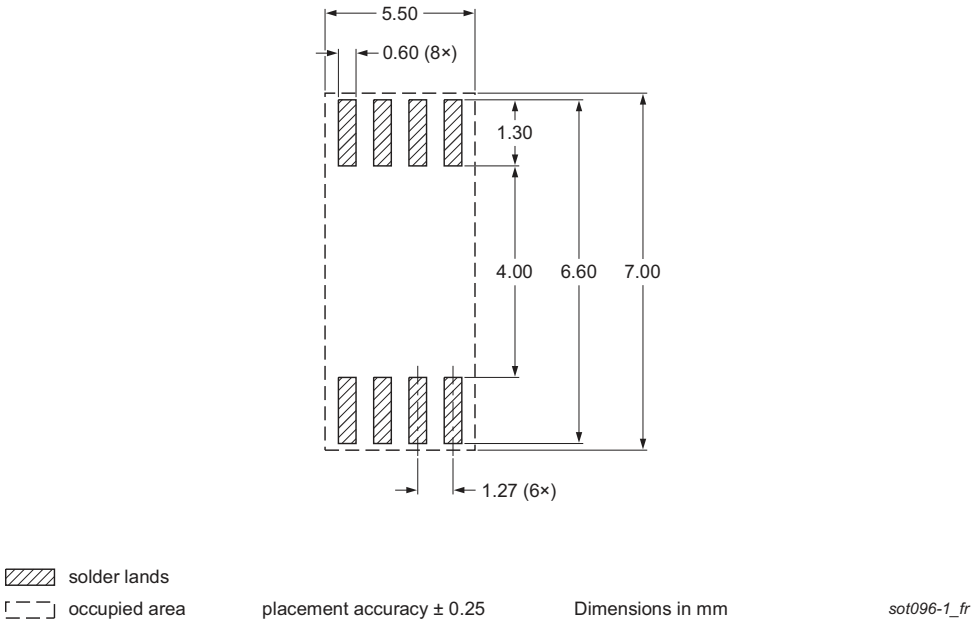

Fig 18. PCB footprint for SOT96-1 (SO8); reflow soldering

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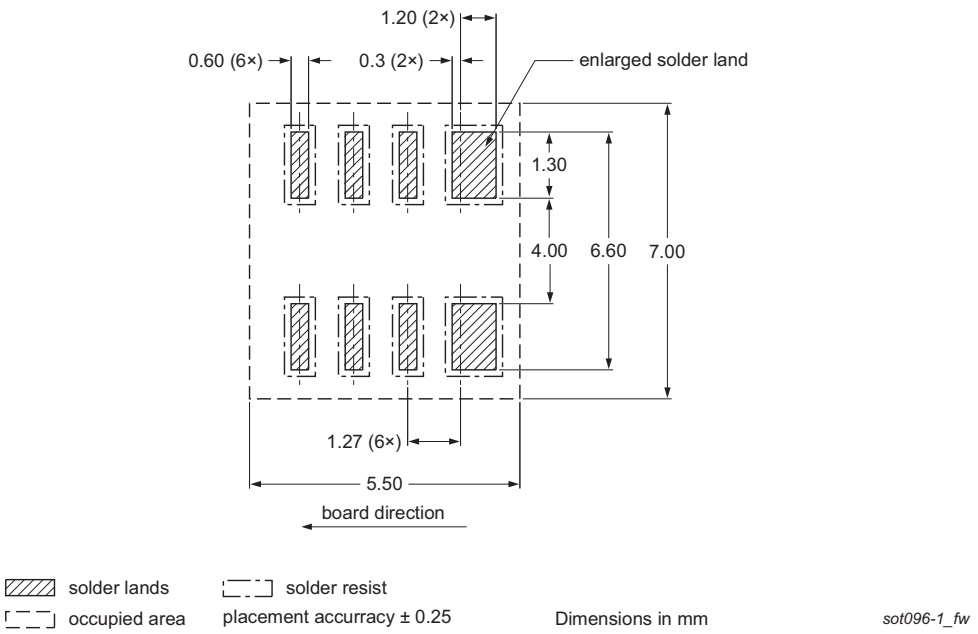

Fig 19. PCB footprint for SOT96-1 (SO8); wave soldering

17. Abbreviations

Table 9. Abbreviations

Acronym	Description
FET	Field-Effect Transistor
HF	High Frequency
IF	Intermediate Frequency
LAN	Local Area Network
LO	Local Oscillator
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
RF	Radio Frequency
S/N	Signal-to-Noise ratio
VHF	Very High Frequency

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18. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA612A v.3	20140604	Product data sheet	-	SA612A v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 “General description”, last sentence: deleted “8-lead dual in-line plastic package” • Table 1 “Ordering information”: – Type number SA612AN (DIP8 package, SOT97-1 package outline) is discontinued and removed from this data sheet – Type number changed from “SA612AD” to “SA612AD/01” • Added Section 4.1 “Ordering options” • Figure 2 “Pin configuration for SO8”, pin names are updated: – Pin 1: from “INPUT A” to “IN_A” – Pin 2: from “INPUT B” to “IN_B” – Pin 4: from “OUTPUT A” to “OUT_A” – Pin 5: from “OUTPUT B” to “OUT_B” – Pin 6: from “OSCILLATOR” to “OSC_B” – Pin 7: from “OSCILLATOR” to “OSC_E” • Added Section 6.2 “Pin description” • Section 7 “Functional description”, seventh paragraph, second sentence changed from “In this circuit, a third overtone parallel-mode crystal with approximately 5 pF load capacitance should be specified.” to “As shown, an overtone mode of operation is utilized.” • Figure 7 “Colpitts oscillator suitable for synthesizer applications and typical buffers”: capacitor value corrected from “0.10 pF” to “10 nF” (above pin 8) • Old table “AC/DC electrical characteristics” split into Table 5 “Static characteristics” and Table 6 “Dynamic characteristics” • Table 6 “Dynamic characteristics”, Conditions for $IP3_i$, input third-order intercept point, updated from “at 45 MHz; RF input = –45 dBm” to “” • Package outline SOT97-1 (DIP8) is deleted • Added soldering information • Added Section 16 “Soldering: PCB footprints” • Added Section 17 “Abbreviations”			
SA612A v.2	19971107	Product specification	853-0391 18662	NE/SA612A v.1
NE/SA612A v.1	19900917	Product specification	853-0391 00446	-

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19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 4 June 2014
Document identifier: SA612A

Microphone Preamplifier with Variable Compression and Noise Gating

SSM2165*

FEATURES

Complete Microphone Conditioner in an 8-Lead Package
Single 5 V Operation
Preset Noise Gate Threshold
Compression Ratio Set by External Resistor
Automatic Limiting Feature Prevents ADC Overload
Adjustable Release Time
Low Noise and Distortion
20 kHz Bandwidth (±1 dB)
Low Cost

APPLICATIONS

Microphone Preamplifier/Processor
Computer Sound Cards
Public Address/Paging Systems
Communication Headsets
Telephone Conferencing
Guitar Sustain Effects Generator
Computerized Voice Recognition
Surveillance Systems
Karaoke and DJ Mixers

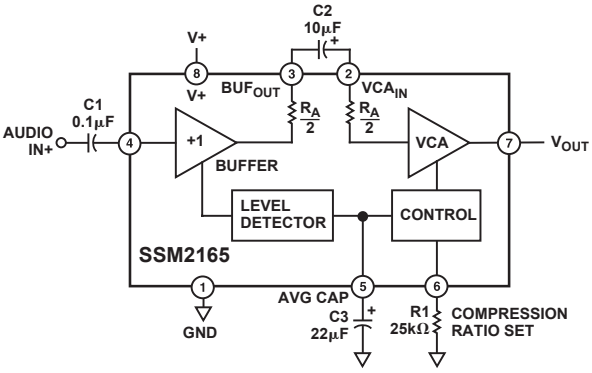
GENERAL DESCRIPTION

The SSM2165 is a complete and flexible solution for conditioning microphone inputs in computer audio systems. It is also excellent for improving vocal clarity in communications and public address systems. A low noise voltage controlled amplifier (VCA) provides a gain that is dynamically adjusted by a control loop to maintain a set compression characteristic. The compression ratio is set by a single resistor and can be varied from 1:1 to over 15:1 relative to the fixed rotation point. Signals above the rotation point are limited to prevent overload and to eliminate "popping." A downward expander (noise gate) prevents amplification of noise or hum. This results in optimized signal levels prior to digitization, thereby eliminating the need for additional gain or attenuation in the digital domain that could add noise or impair accuracy of speech recognition algorithms. The flexibility of setting the compression ratio and the time constant of the level detector, coupled with two values of rotation point, make the SSM2165 easy to integrate in a wide variety of microphone conditioning applications.

The SSM2165 is an ideal companion product for audio codecs used in computer systems, such as the AD1845 and AD1847. The device is available in 8-lead SOIC and P-DIP packages, and guaranteed for operation over the extended industrial temperature range of –40°C to +85°C. As shown in Figure 1a, the SSM2165-1 has a rotation point of –25.7 dBu (40 mV)[1], a VCA gain of 18 dB, and gives –7.7 dBu (320 mV) before limiting. As shown in Figure 1b, the SSM2165-2 has a rotation point of –17.8 dBu (100 mV), a VCA gain of 8 dB and gives –9.8 dBu (250 mV) before limiting. Both have a noise gate threshold of –64 dBu (500 μV), below which downward expansion reduces the gain with a ratio of approximately 1:3. That is, a –3 dB reduction of output signal occurs with a –1 dB reduction of input signal. For applications requiring adjustable noise gate threshold, VCA gain up to 18 dB, and adjustable rotation point, please refer to the SSM2166.

*Patents pending.
[1]All signals are in rms volts or dBu (0 dBu = 0.775 V rms).

FUNCTIONAL BLOCK DIAGRAM



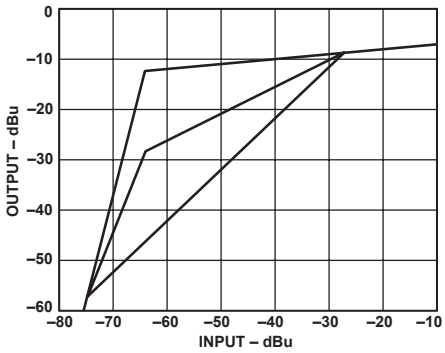


Figure 1a. SSM2165-1 Compression and Gating Characteristics

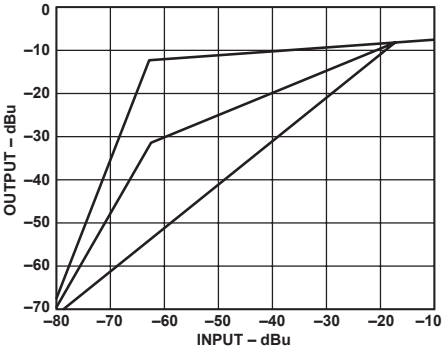


Figure 1b. SSM2165-2 Compression and Gating Characteristics

REV. B

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SSM2165–SPECIFICATIONS (V+ = 5 V, f = 1 kHz, R_L = 100 kΩ, R_{COMP} = 0 Ω, T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUDIO SIGNAL PATH						
Voltage Noise Density	e_n	15:1 Compression, V_{IN} = GND		17		nV/√Hz[2]
Noise		20 kHz Bandwidth, V_{IN} = GND		–109		dBu[1]
Total Harmonic Distortion	THD+N					
SSM2165-1		2nd and 3rd Harmonics, V_{IN} = –30 dBu		0.2	0.5	%
SSM2165-2		2nd and 3rd Harmonics, V_{IN} = –20 dBu		0.2	0.5	%
		22 kHz Low-Pass Filter				
Input Impedance	Z_{IN}			180		kΩ
Output Impedance	Z_{OUT}			75		Ω
Load Drive		Resistive	5			kΩ
		Capacitive			2	nF
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1.4		V rms
Gain Bandwidth Product		1:1 Compression				
SSM2165-1		VCA G = 18 dB		300		kHz
SSM2165-2		VCA G = 8 dB		100		kHz
CONTROL SECTION						
VCA Dynamic Gain Range				40		dB
VCA Fixed Gain						
SSM2165-1				18		dB
SSM2165-2				8		dB
Rotation Point						
SSM2165-1				40		mV rms
SSM2165-2				100		mV rms
Compression Ratio, Min				1:1		
Compression Ratio, Max				15:1		
Control Feedthrough		15:1 Compression		±5		mV
POWER SUPPLY						
Supply Voltage Range	V_S		4.5		5.5	V
Supply Current	I_{SY}			7.5	10	mA
Quiescent Output Voltage Level				2.2		V
Power Supply Rejection Ratio[2]	PSRR			50		dB

NOTES
[1]0 dBu = 0.775 V rms.
[2]Referred to input.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . 10 V
Audio Input Voltage . . . . . Supply Voltage
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

ESD RATINGS

883 (Human Body) Model . . . . . 2.0 kV

THERMAL CHARACTERISTICS

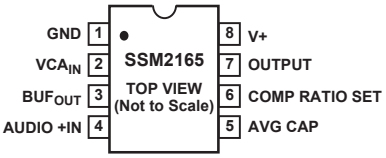
Thermal Resistance
8-Lead Plastic DIP
θ_{JA} . . . . . 103°C/W
θ_{JC} . . . . . 43°C/W
8-Lead SOIC
θ_{JA} . . . . . 158°C/W
θ_{JC} . . . . . 43°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
SSM2165-1P*	–40°C to +85°C	Plastic DIP	N-8
SSM2165-1S	–40°C to +85°C	Narrow SOIC	SO-8
SSM2165-2S	–40°C to +85°C	Narrow SOIC	SO-8

*Not for new design, obsolete April 2002.

PIN CONFIGURATION



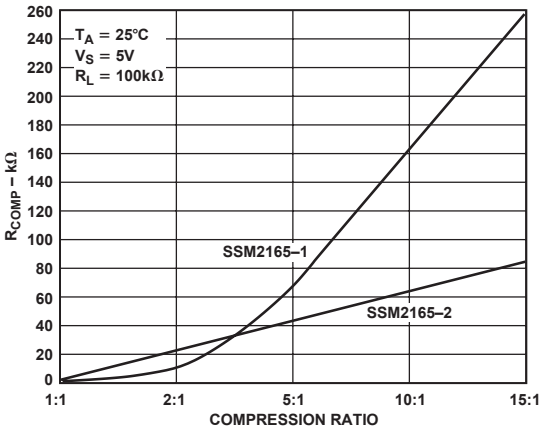
PIN FUNCTION DESCRIPTIONS

Pin #	Mnemonic	Function
1	GND	Ground
2	VCA$_{IN}$	VCA Input Pin. A typical connection is a 1 µF–10 µF capacitor from the buffer output pin (Pin 3) to this pin.
3	BUF$_{OUT}$	Input Buffer Amplifier Output Pin. Must not be loaded by capacitance to ground.
4	AUDIO +IN	Input Audio Signal. The input signal should be ac-coupled (0.1 µF typical) into this pin.
5	AVG CAP	Detector Averaging Capacitor. A capacitor, 2.2 µF–22 µF, to ground from this pin is the averaging capacitor for the detector circuit.
6	COMP RATIO SET	Compression Ratio Set Pin. A resistor to ground from this pin sets the compression ratio as shown in TPC 1.
7	OUTPUT	Output Signal.
8	V+	Positive Supply, 5 V Nominal.

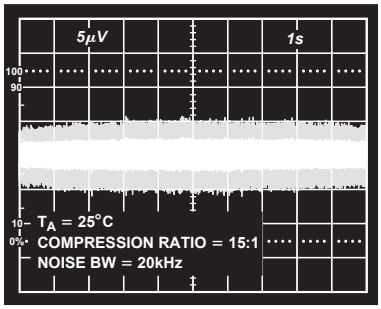
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2165 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

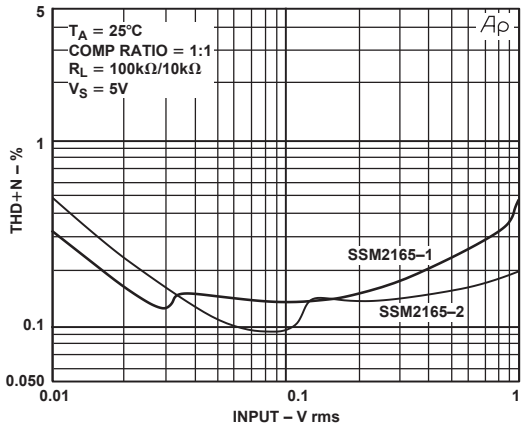
SSM2165–Typical Performance Characteristics



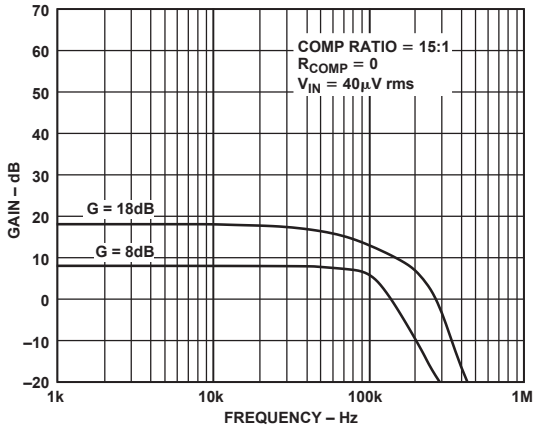
TPC 1. Compression Ratio vs. R_{COMP}



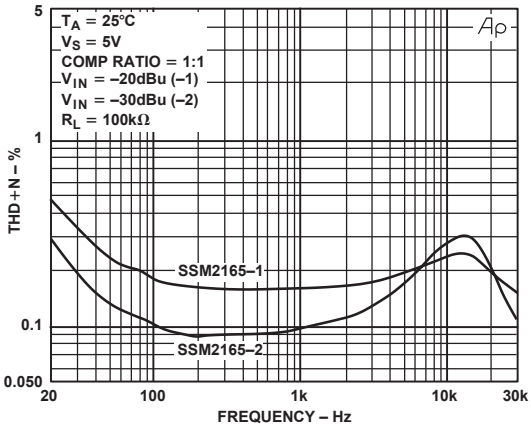
TPC 4. Wideband Output Noise



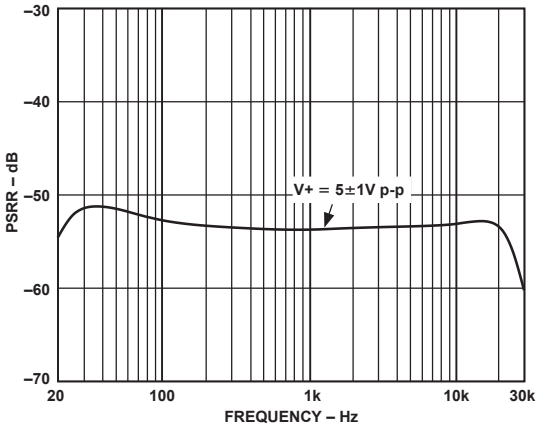
TPC 2. THD + N (%) vs. Input (V rms)



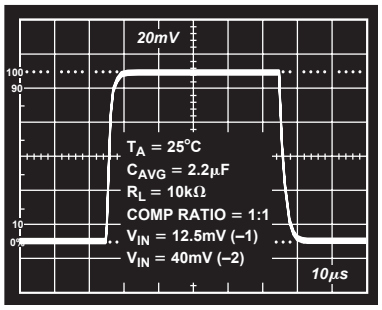
TPC 5. GBW Curves vs. VCA Gain



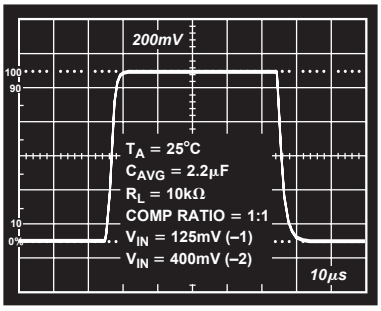
TPC 3. THD + N (%) vs. Frequency (Hz)



TPC 6. PSRR vs. Frequency, Referred to Input



TPC 7. Small Signal Transient Response



TPC 8. Large Signal Transient Response

APPLICATIONS INFORMATION

The SSM2165 is a complete microphone signal conditioning system in a single integrated circuit. Designed primarily for voiceband applications, this integrated circuit provides amplification, rms detection, limiting, variable compression, and downward expansion. The internal rms detector has a time constant set by an external capacitor. An integral voltage-controlled amplifier (VCA) provides up to 40 dB of gain in the signal path with approximately 30 kHz bandwidth. The device operates on a single 5 V supply, accepts input signals up to 1 V[1], and produces output signal levels at limiting of 320 mV and 250 mV for the SSM2165-1 and SSM2165-2 respectively, into loads > 5 kΩ.

The SSM2165 contains an input buffer and automatic gain control (AGC) circuit for audio and voice band signals. Circuit operation is optimized by providing user-adjustable compression ratio and time constant. A downward expansion (noise gating) feature reduces background and circuit noise below 500 μV. The rotation point determines the output signal levels before limiting (referred to the input), and is 40 mV for the SSM2165-1 and 100 mV for the SSM2165-2.

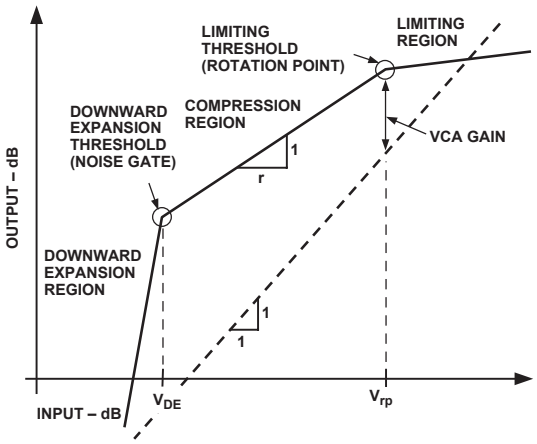


Figure 2. General Input/Output Characteristics of the SSM2165

[1]All signals are in rms volts or dBu (0 dBu = 0.775 V rms).

THEORY OF OPERATION

Figure 2 illustrates the general transfer characteristic for the SSM2165 where the output level in dBu is plotted as a function of the input level in dBu (0 dBu = 0.775 V rms). For input signals in the range of V_{DE} (Downward Expansion) to V_{RP} (Rotation Point) an "r" dB change in the input level causes a 1 dB change in the output level. Here, "r" is defined as the "compression ratio." The compression ratio may be varied from 1:1 (no compression) to over 15:1 via a single resistor, R_{COMP}. Input signals above V_{RP} are compressed with a fixed compression ratio of approximately 10:1. This region of operation is the "limiting region." Varying the compression ratio has no effect on the limiting region. The breakpoint between the compression region and the limiting region is referred to as the "limiting threshold" or "rotation point," and is different for the SSM2165-1 and SSM2165-2, see Table I.

Table I. Characteristics vs. Dash Number

SSM2165	Rotation Point	Gain	Output*
–1	40 mV (–25.7 dBu)	18 dB	320 mV (–6 dBu)
–2	100 mV (–17.7 dBu)	8 dB	250 mV (–8 dBu)

*At limiting.

The term "rotation point" derives from the observation that the straight line in the compression region "rotates" about this point on the input/output characteristic as the compression ratio is changed.

When the compression is set to 2:1, a –2 dB change of the input signal level in the compression region causes –1 dB change of the output level. Likewise, at 10:1 compression, a –10 dB change of the input signal level in the compression region causes a –1 dB change in the output level. The gain of the system with an input signal level of V_{RP} is fixed regardless of the compression ratio, and is different for the SSM2165-1 and SSM2165-2 (see Figures 1a and 1b). The "nominal gain" of the system is 18 dB for the SSM2165-1, and 8 dB for the SSM2165-2. System gain is measured at V_{RP} and is ($V_{OUT} - V_{IN}$) in dB.

Input signals below V_{DE} are downward expanded at a ratio of approximately 1:3. As a result, the gain of the system is small for very small input signal levels below V_{DE}, even though it may be quite large for input signals above V_{DE}. The downward expansion threshold, V_{DE}, is fixed at 500 μV (–64 dBu) for both dash versions.

The SSM2165 Signal Path

Figure 3 illustrates the block diagram of the SSM2165. The audio input signal is processed by the unity gain input buffer and then by the VCA. The buffer presents an input impedance of approximately 180 kΩ to the source. A dc voltage of approximately 1.5 V is present at AUDIO +IN (Pin 4), requiring the use of a blocking capacitor (C1) for ground-referenced sources. A 0.1 µF capacitor is a good choice for most audio applications. The buffer is designed to drive only the low impedance input of the VCA, and must not be loaded by capacitance to ground. The VCA is a low distortion, variable-gain amplifier whose gain is set by the internal control circuitry. The input to the VCA is a virtual ground in series with 500 Ω. An external blocking capacitor (C2) must be used between the buffer's output and the VCA input. The desired low frequency response and the total of 1 kΩ impedance between amplifiers determine the value of this capacitor. For music applications, 10 µF will give high pass f_C = 16 Hz. For voice/communications applications, 1 µF will give f_C = 160 Hz. An aluminum electrolytic capacitor is an economical choice. The VCA amplifies the input signal current flowing through C6 and converts this current to a voltage at the SSM2165's output (Pin 7). The net gain from input to output can be as high as 40 dB for high compression ratios and depending on the gain set by the control circuitry. The output impedance of the SSM2165 is typically less than 75 Ω, and the external load on Pin 7 should be >5 kΩ. The nominal output dc voltage of the device is approximately 2.2 V. Use a dc blocking capacitor for grounded loads.

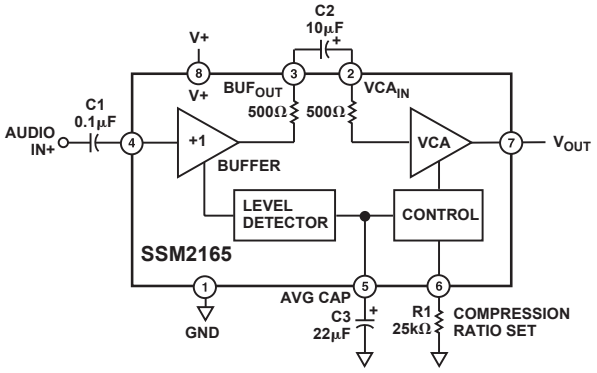


Figure 3. Functional Block Diagram and Typical Voice Application

The bandwidth of the SSM2165 is quite wide at all gain settings. The upper –3 dB point is approximately 300 kHz. The GBW plots are shown in TPC 5. While the noise of the input buffer is fixed, the input referred noise of the VCA is a function of gain. The VCA input noise is designed to be a minimum when the gain is at a maximum, thereby optimizing the usable dynamic range of the part. A photograph of the SSM2165's wideband peak-to-peak output noise is illustrated in TPC 4.

The Level Detector

The SSM2165 incorporates a full-wave rectifier and a patent-pending, true rms level detector circuit whose averaging time constant is set by an external capacitor connected to the AVG CAP pin (Pin 5). Capacitor values from 18 µF to 22 µF have been found to be more appropriate in voiceband applications, where capacitors on the low end of the range seem more appropriate for music program material. For optimal low frequency operation of the level detector down to 10 Hz, the value of the capacitor should be around 22 µF. Some experimentation with larger values for the AVG CAP may be necessary to reduce the effects of excessive low frequency ambient background noise. The value of the averaging capacitor affects sound quality: too small a value for this capacitor may cause a "pumping effect" for some signals, while too large a value can result in slow response times to signal dynamics. Electrolytic capacitors are recommended here for lowest cost.

The rms detector filter time constant is approximately given by $10 \times C_{AVG}$ milliseconds where C_{AVG} is in µF. This time constant controls both the steady-state averaging in the rms detector as well as the release time for compression, that is, the time it takes for the system gain to react when a large input is followed by a small signal. The attack time, the time it takes for the gain to be reduced when a small signal is followed by a large signal, is mainly controlled by internal circuitry that speeds up the attack for large level changes, and controlled partly by the AVG CAP value. This limits overload time to under 1 ms in most cases.

The performance of the rms level detector is illustrated in Figure 4 for C_{AVG} = 2.2 µF and Figure 5 for C_{AVG} = 22 µF. In each of these photographs, the input signal to the SSM2165 (not shown) is a series of tone bursts in six successive 10 dB steps. The tone bursts range from –66 dBu (0.5 mV rms) to –6 dBu (0.5 V rms). As illustrated in the photographs, the attack time of the rms level detector is dependent only on C_{AVG}, but the release times are linear ramps whose decay times are dependent on both for C_{AVG} and the input signal step size. The rate of release is approximately 240 dB/s for a C_{AVG} = 2.2 µF, and 12 dB/s for a C_{AVG} of 22 µF.

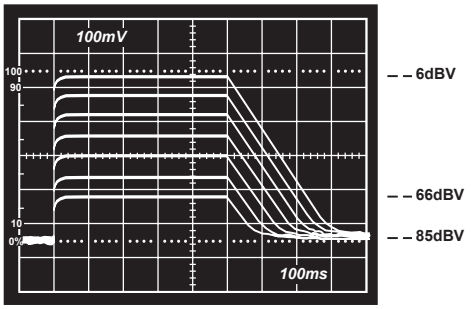


Figure 4. RMS Level Detector Performance with C_{AVG} = 2.2 µF

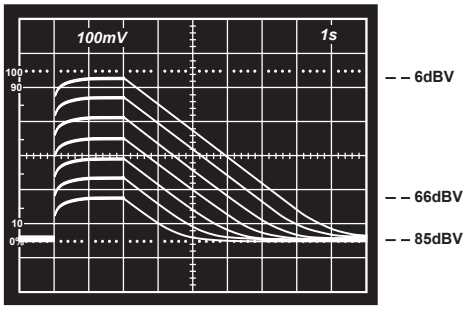


Figure 5. RMS Level Detector Performance with C_{AVG} = 22 µF

Control Circuitry
The output of the rms level detector is a signal proportional to the log of the true rms value of the buffer output with an added dc offset. The control circuitry subtracts a dc voltage from this signal, scales it, and sends the result to the VCA to control the gain. The VCA's gain control is logarithmic: a linear change in control signal causes a dB change in gain. It is this control law that allows linear processing of the log rms signal to provide the flat compression characteristic on the input/output characteristic shown in Figure 2.

Compression Ratio
Changing the scaling of the control signal fed to the VCA causes a change in the circuit's compression ratio, "r." This effect is shown in Figure 6. The compression ratio can be set by connecting a resistor between the COMP RATIO pin (Pin 6) and GND. Lowering RCOMP gives smaller compression ratios as indicated in TPC 1, with values of about 5 kΩ or less resulting in a compression ratio of 1:1. AGC performance is achieved with compression ratios between 2:1 and 15:1, and is dependent on the application. A 200 kΩ potentiometer may be used to allow this parameter to be adjusted.

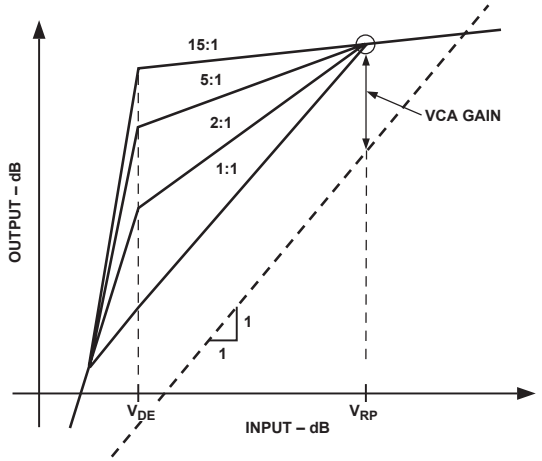


Figure 6. Effect of Varying the Compression Ratio

Rotation Point
An internal dc reference voltage in the control circuitry sets the rotation point. The rotation point determines the output level above which limiting occurs. That is, in the limiting region, a 10 dB change of input results in a 1 dB change of output. The rotation point is set to 40 mV (–26 dBu) for the SSM2165-1 and 100 mV (–18 dBu) for the SSM2165-2. In the SSM2165, limiting is compression at a fixed compression ratio of approximately 15:1. The fixed gain in the VCA is 18 dB for the SSM2165-1 and 8 dB for the SSM2165-2. The output signals at limiting are, therefore, 320 mV and 250 mV respectively. These are summarized in Table I.

Maximum Output
Since limiting occurs for signals larger than the rotation point ($V_{IN} > V_{RP}$), the rotation point effectively sets the maximum output signal level. The application will determine which version of the SSM2165 should be selected. The output level should match the maximum input allowed by the following stage. Occasional larger signal transients will then be attenuated by the action of the limiter.

Downward Expansion Threshold
The downward expansion threshold, or noise gate, is determined by a reference voltage internal to the control circuitry. The noise gate threshold is 500 µV for both versions of the SSM2165. Users requiring some other noise gate should consider using the SSM2166. High volume users may wish to consider a custom version of the SSM2165 with other noise gate thresholds or rotation points.

Power-On/Power-Off Settling Time
Cycling the power supply to the SSM2165 will result in quick settling times: the off-on settling time of the SSM2165 is less than 200 ms, while the on-off settling time is less than 1 ms. Note that transients may appear at the output of the device during power up and power down. A clickless mute function is available on the SSM2166 only.

PC Board Layout Considerations
Since the SSM2165 is capable of wide bandwidth operation at high gain, special care must be exercised in the layout of the PC board which contains the IC and its associated components. The following applications hints should be considered and/or followed:

1. In some high system gain applications, the shielding of input wires to minimize possible feedback from the output of the SSM2165 back to the input circuit may be necessary.
2. A single-point ("star") ground implementation is recommended in addition to maintaining short lead lengths and PC board runs. In systems where an analog ground and a digital ground are available, the SSM2165 and its surrounding circuitry should be connected to the analog ground. Wire-wrap board connections and grounding implementations are to be explicitly avoided.
3. The internal buffer of the SSM2165 was designed to drive only the input of the internal VCA and its own feedback network. Stray capacitive loading to ground from either Pin 3 or Pin 2 in excess of 5 pF to 10 pF can cause excessive phase shift and can lead to circuit instability.
4. When using high impedance sources, it can be advantageous to shunt the source with a capacitor to ground at the input pin of the IC (Pin 4) to lower the source impedance at high frequencies, as shown in Figure 7. A capacitor with a value of 1000 pF is a good starting value and sets a low pass corner at 31 kHz for 5 kΩ sources.

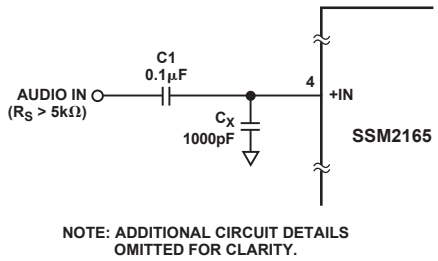


Figure 7. Circuit Configuration for Use with High Impedance Signal Sources

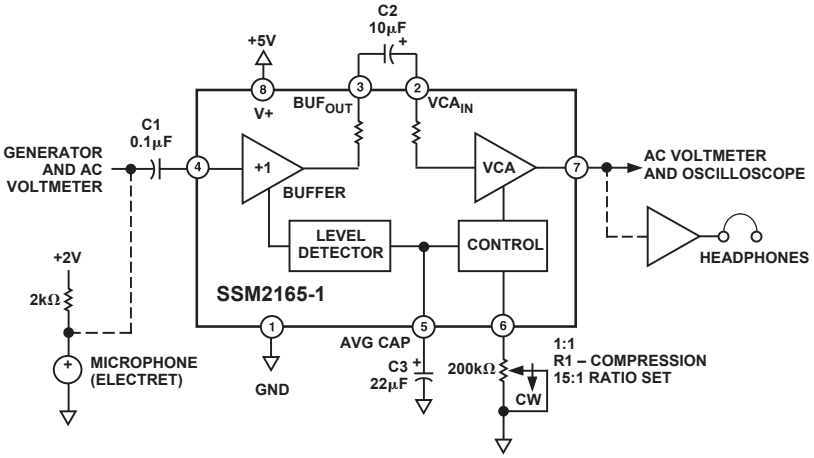


Figure 8. Electret Microphone Preamp Example

Compression Adjustment—A Practical Example

To illustrate how to set the compression ratio of the SSM2165, we will take a practical example. The SSM2165 will be used interface an electret-type microphone to a post-amplifier, as shown in Figure 8. The signal from the microphone was measured under actual conditions to vary from 2 mV to 30 mV. The post-amplifier requires no more than 350 mV at its input. We will, therefore, choose the SSM2165-1, whose "rotation" point is 40 mV and whose VCA fixed gain is 18 dB (×8), thus giving 320 mV at limiting. From prior listening experience, we will use a 2:1 compression ratio. The noise gate threshold of the SSM2165-1 will operate when the input signal falls below 500 µV. These objectives are summarized in Table II. The transfer characteristic we will implement is illustrated in Figure 10.

Table II. Objective Specification of Example

Input Range	2 mV–30 mV
Output Range	To 350 mV
Limiting Level	320 mV
Compression	2:1
Gain	18 dB
Noise Gate	500 µV

Test Equipment Setup

The recommended equipment and configuration is shown in Figure 9. A low noise audio generator with a smooth output adjustment range of 100 µV to 25 mV is a suitable signal source. The output voltmeter should go up to 2 V. The oscilloscope is used to verify that the output is sinusoidal, that no clipping is occurring in the buffer, and to observe the limiting and noise gating "knees."

Breadboard Considerations

When building a breadboard, keep the leads to Pins 2 and 3 as short as possible. Use a central analog ground and decouple power supply connections adequately.

Figure 9. Test Equipment Setup

STEP 1. Initialize Potentiometer

With power off, preset R1—Compression Ratio potentiometer to zero ohms.

STEP 2. Check Setup

With power on, adjust the generator for an input level of 50 mV (–24 dBu), 1 kHz. The output meter should indicate approximately 350 mV (–6.9 dBu). If not, check the setup.

STEP 3. Find the Rotation Point

Set the input level to 50 mV (–24 dBu), and observe the output on the oscilloscope. The output will be in the limiting range of operation. Slowly reduce the input signal level until the output level just begins to stop limiting and follows the input down. Increase the input so that the output is 320 mV (–7.7 dBu). This is the knee of the rotation point.

STEP 4. Adjust the Compression Ratio

With the input set as in Step 3, note the exact value of the input signal level just below the knee (around 40 mV (–26 dBu)). Next, reduce the input to 1/4 the value noted, (around 10 mV (–38 dBu)), for a change of –12 dB. Next, increase the R_{COMP} potentiometer resistance so the output is 160 mV (–13.7 dBu) for an output change of –6 dB. You have now set the compression, which is the ratio of input change to output change, in dB, to 2:1.

STEP 5. Confirm the Noise Gate Threshold

Set the input to 1 mV, and observe the output on the oscilloscope. A 20 dB pad between generator and input may facilitate this measurement. Reduce the input gradually until the output falls off more rapidly. This point is the noise gate threshold, and should be approximately 500 µV (–64 dBu). The noise gate threshold on the SSM2165 is fixed at 500 µV, a practical value for many microphones. Should a different noise gate threshold be required, consider using the SSM2166.

STEP 6. Listen

At this time the signal generator may be replaced with a properly powered electret microphone and listen to the results through a set of headphones. The microphone's internal FET usually requires around 2 V through a 2 kΩ resistor; this varies with the manufacturer. Experiment with the compression ratio value and averaging capacitor size. More compression will keep the output steady over a wider range of microphone-to-source distance. Varying the averaging capacitor, C_{AVG}, changes the rms detector averaging time, and the decay time of the gate. Both compression ratio and decay time are usually determined by critical listening to the intended audio input.

STEP 7. Record Values

With the power removed from the test fixture, measure and record the values of the R_{COMP} and $C_{AVG.}$

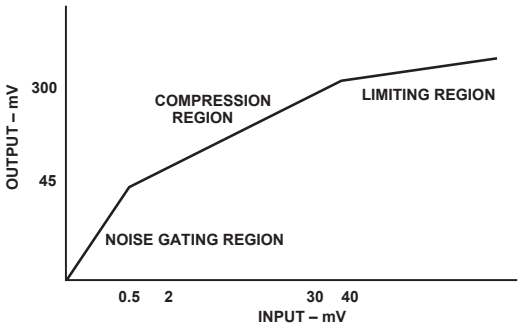


Figure 10. Transfer Characteristic

SUMMARY

We have implemented the transfer characteristic of Figure 10. For inputs below the 500 µV noise gate threshold, circuit and background noise will be downward expanded (gain-reduced) at a ratio of approximately 1:3. That is, a –1 dB change in the noise will result in –3 dB decrease at the output. Above threshold, the signal will increase at a rate of 1 dB for each 2 dB input increase, until the rotation point is reached at an input of approximately 40 mV. In the limiting region, the compression ratio increases to approximately 15:1. That is, a 15 dB increase in input will produce a 1 dB increase at the output, so there will be little further increase for higher level inputs.

Other Versions

The SSM2165 is an 8-lead version of the 14-lead SSM2166 which is recommended for applications requiring more versatility. The SSM2166 allows selection of noise gate threshold and rotation point, and allows the buffer to provide up to 20 dB of gain. Power-down and mute functions are also built in. Customized versions of the SSM2165 are available for large volume users. The wide dynamic range of the SSM2165 makes it useful in many applications other than microphone signal conditioning such as a sustain generator for guitars. For further information, contact your Analog Devices representative.

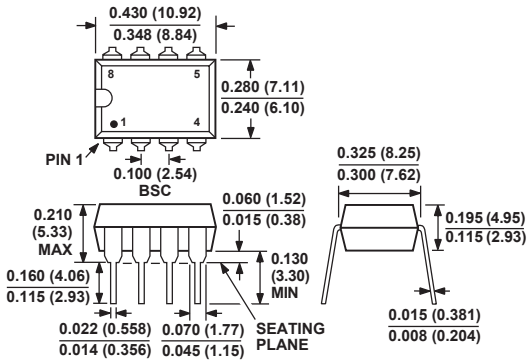
Revision History

Location	Page
Data Sheet changed from REV. A to REV. B.	
Edits to ORDERING GUIDE	3

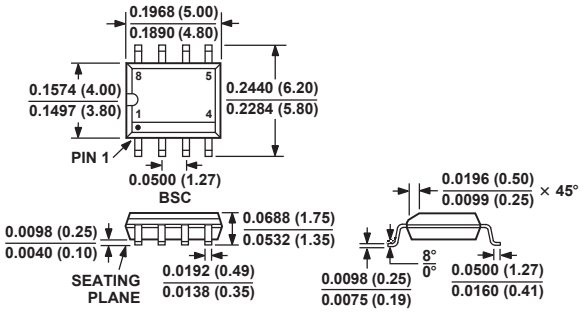
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead Narrow-Body SOIC (SO-8)



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C00356-0-1/02(B)

LM386 Low Voltage Audio Power Amplifier

1 Features

- Battery Operation
- Minimum External Parts
- Wide Supply Voltage Range: 4 V–12 V or 5 V–18 V
- Low Quiescent Current Drain: 4 mA
- Voltage Gains from 20 to 200
- Ground-Referenced Input
- Self-Centering Output Quiescent Voltage
- Low Distortion: 0.2% (A_V = 20, V_S = 6 V, R_L = 8 Ω, P_O = 125 mW, f = 1 kHz)
- Available in 8-Pin MSOP Package

2 Applications

- AM-FM Radio Amplifiers
- Portable Tape Player Amplifiers
- Intercoms
- TV Sound Systems
- Line Drivers
- Ultrasonic Drivers
- Small Servo Drivers
- Power Converters

3 Description

The LM386M-1 and LM386MX-1 are power amplifiers designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

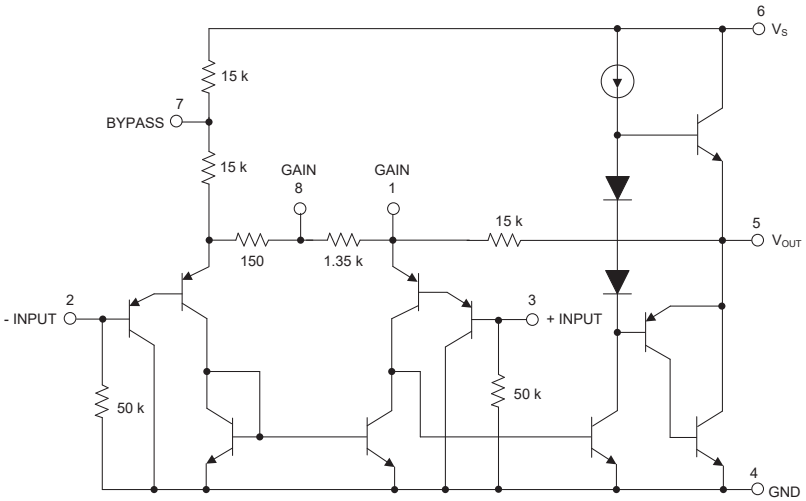
The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 mW when operating from a 6-V supply, making the LM386M-1 and LM386MX-1 ideal for battery operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM386N-1	PDIP (8)	9.60 mm × 6.35 mm
LM386N-3	PDIP (8)	9.60 mm × 6.35 mm
LM386N-4	PDIP (8)	9.60 mm × 6.35 mm
LM386M-1	SOIC (8)	4.90 mm × 3.90 mm
LM386MX-1	SOIC (8)	4.90 mm × 3.90 mm
LM386MMX-1	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2017) to Revision C	Page
• Changed devices LM386M-1/LM386MX-1 To: LM386 in the data sheet title	1
• Changed From: LM386N-4 To: Speaker Impedance in the *Recommended Operating Conditions* table	4
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 1	8
• Changed kW To: kΩ in the *Gain Control* section	8
• Changed kW To: kΩ in the *Input Biasing* section	9
• Changed Figure 11	9
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 2	10
• Changed Figure 13	10
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 3	11
• Changed Figure 15	11
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 4	12
• Changed Figure 17	12
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 5	13
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 6	14
• Changed Figure 21	14
• Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in Table 7	15
• Changed Figure 23	15

Changes from Revision A (May 2004) to Revision B	Page
• Added LM386MX-1 device to the data sheet.	1
• Added Device Information, Application and Implementation, Power Supply Recommendation, Layout, and Device and Documentation Support sections	1
• Inserted Functional Block Diagram	7

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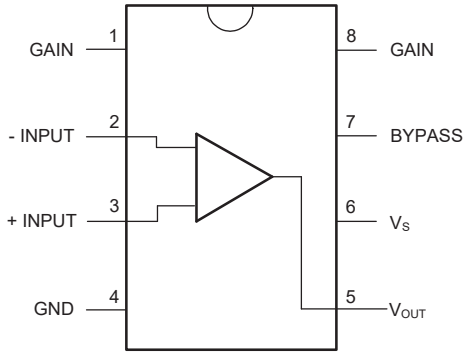
5 Pin Configuration and Functions

D Package
8-Pin MSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GAIN	1	–	Gain setting pin
–INPUT	2	I	Inverting input
+INPUT	3	I	Noninverting input
GND	4	P	Ground reference
V_{OUT}	5	O	Output
V_S	6	P	Power supply voltage
BYPASS	7	O	Bypass decoupling path
GAIN	8	–	Gain setting pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage, V_{CC}	LM386N-1/-3, LM386M-1		15	V
	LM386N-4		22	
Package Dissipation	LM386N		1.25	W
	LM386M		0.73	
	LM386MM-1		0.595	
Input Voltage, V_I		–0.4	0.4	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4		12	V
	LM386N-4	5		18	V
	Speaker Impedance	4			Ω
VI	Analog input voltage	–0.4		0.4	V
TA	Operating free-air temperature	0		70	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM386 D (SOIC) 8	LM386 DGK (VSSOP) 8	LM386 P (PDIP) 8	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.7	169.3	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.7	73.1	42.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.2	100.2	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.4	9.2	19.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.6	99.1	50.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S	Operating Supply Voltage	LM386N-1, -3, LM386M-1, LM386MM-1	4		12	V
		LM386N-4	5		18	
I_Q	Quiescent Current	V_S = 6 V, V_{IN} = 0		4	8	mA
P_{OUT}	Output Power	V_S = 6 V, R_L = 8 Ω, THD = 10% (LM386N-1, LM386M-1, LM386MM-1)	250	325		mW
		V_S = 9 V, R_L = 8 Ω, THD = 10% (LM386N-3)	500	700		
		V_S = 16 V, R_L = 32 Ω, THD = 10% (LM386N-4)	700	100		
A_V	Voltage Gain	V_S = 6 V, f = 1 kHz		26		dB
		10 µF from Pin 1 to 8		46		
BW	Bandwidth	V_S = 6 V, Pins 1 and 8 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 6 V, R_L = 8 Ω, POUT = 125 mW f = 1 kHz, Pins 1 and 8 Open		0.2%		
PSRR	Power Supply Rejection Ratio	V_S = 6 V, f = 1 kHz, CBYPASS = 10 µF Pins 1 and 8 Open, Referred to Output		50		dB
R_{IN}	Input Resistance			50		kΩ
I_{BIAS}	Input Bias Current	V_S = 6 V, Pins 2 and 3 Open		250		nA

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6.6 Typical Characteristics

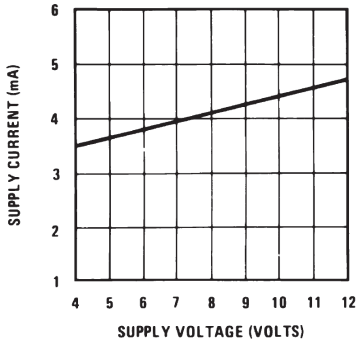

Figure 1. Supply Current vs Supply Voltage

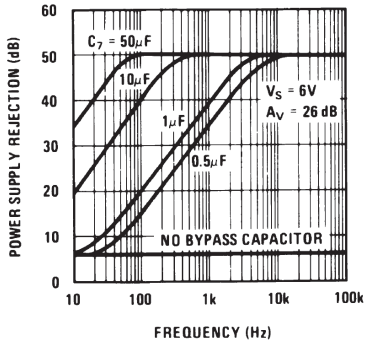

Figure 2. Power Supply Rejection vs Frequency

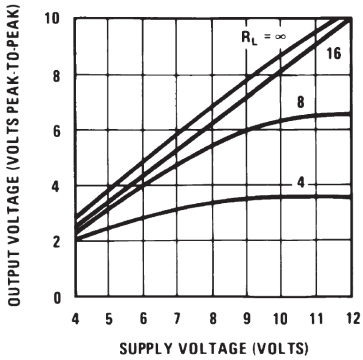

Figure 3. Output Voltage vs Supply Voltage

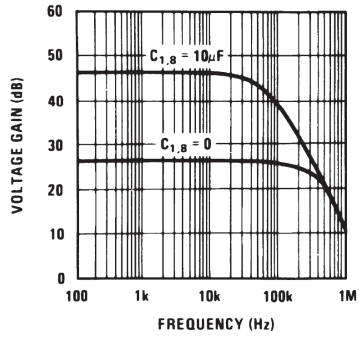

Figure 4. Voltage Gain vs Frequency

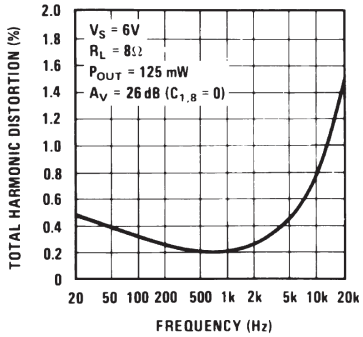

Figure 5. Total Harmonic Distortion vs Frequency

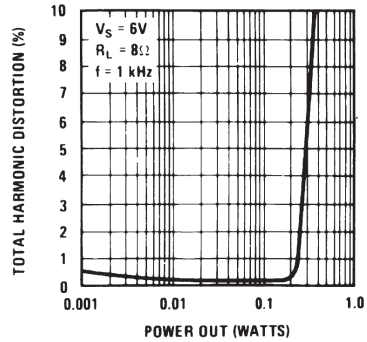

Figure 6. Total Harmonic Distortion vs Power Out

Typical Characteristics (continued)

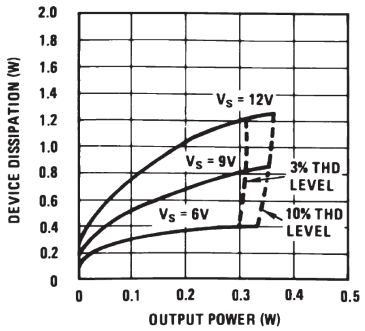

Figure 7. Device Dissipation vs Output Power

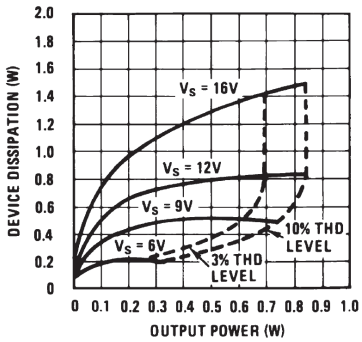

Figure 8. Device Dissipation vs Output Power

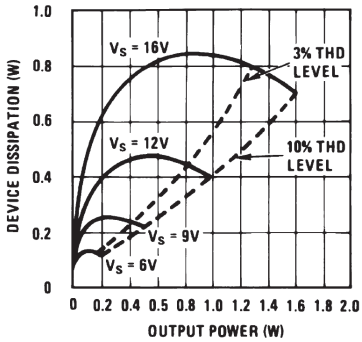

Figure 9. Device Dissipation vs Output Power

7 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

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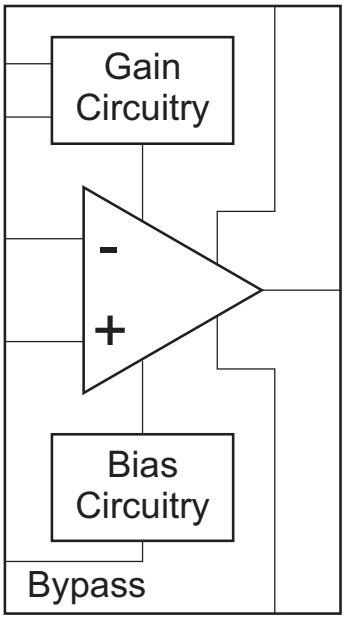
8 Detailed Description

8.1 Overview

The LM386 is a mono low voltage amplifier that can be used in a variety of applications. It can drive loads from 4 Ω to 32 Ω. The gain is internally set to 20 but it can be modified from 20 to 200 by placing a resistor and capacitor between pins 1 and 8. This device comes in three different 8-pin packages as PDIP, SOIC and VSSOP to fit in different applications.

8.2 Functional Block Diagram



8.3 Feature Description

There is an internal 1.35-KΩ resistor that sets the gain of this device to 20. The gain can be modified from 20 to 200. Detailed information about gain setting can be found in the *Detailed Design Procedure* section.

8.4 Device Functional Modes

As this is an Op Amp it can be used in different configurations to fit in several applications. The internal gain setting resistor allows the LM386 to be used in a very low part count system. In addition a series resistor can be placed between pins 1 and 5 to modify the gain and frequency response for specific applications.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Below are shown different setups that show how the LM386 can be implemented in a variety of applications.

9.2 Typical Application

9.2.1 LM386 with Gain = 20

Figure 10 shows the minimum part count application that can be implemented using LM386. Its gain is internally set to 20.

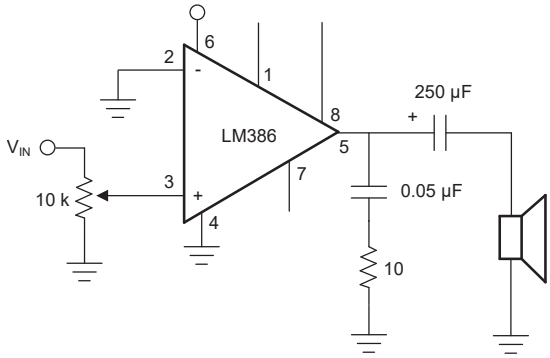


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Figure 10. LM386 with Gain = 20

9.2.1.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Gain Control

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35-kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35-kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15-kΩ resistor). For 6 dB effective bass boost: R ~= 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

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9.2.1.2.2 Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

9.2.1.3 Application Curve

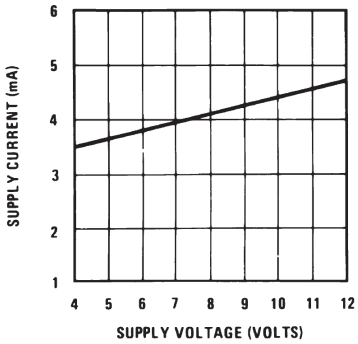

Figure 11. Supply Current vs Supply Voltage

9.2.2 LM386 with Gain = 200

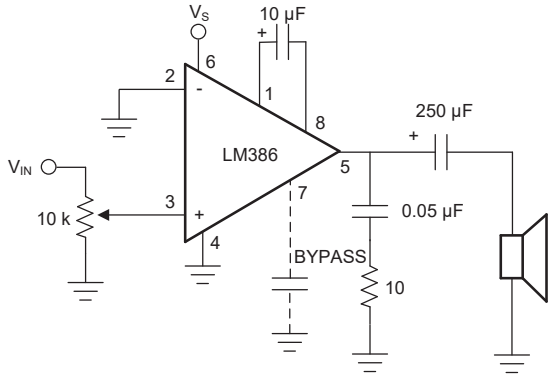

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Figure 12. LM386 with Gain = 200

9.2.2.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.2.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the *Detailed Design Procedure* section.

9.2.2.3 Application Curve

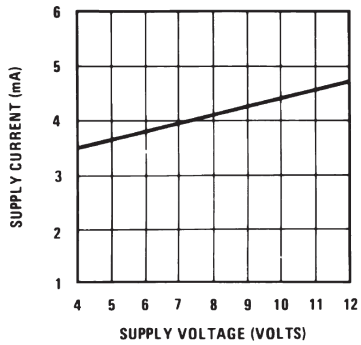

Figure 13. Supply Current vs Supply Voltage

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9.2.3 LM386 with Gain = 50

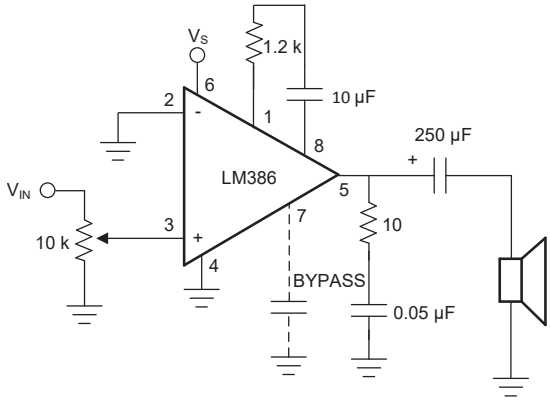

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Figure 14. LM386 with Gain = 50

9.2.3.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.3.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the *Detailed Design Procedure* section.

9.2.3.3 Application Curve

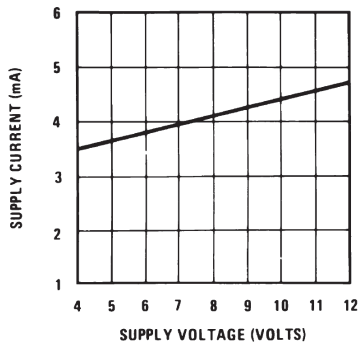

Figure 15. Supply Current vs Supply Voltage

9.2.4 Low Distortion Power Wienbridge Oscillator

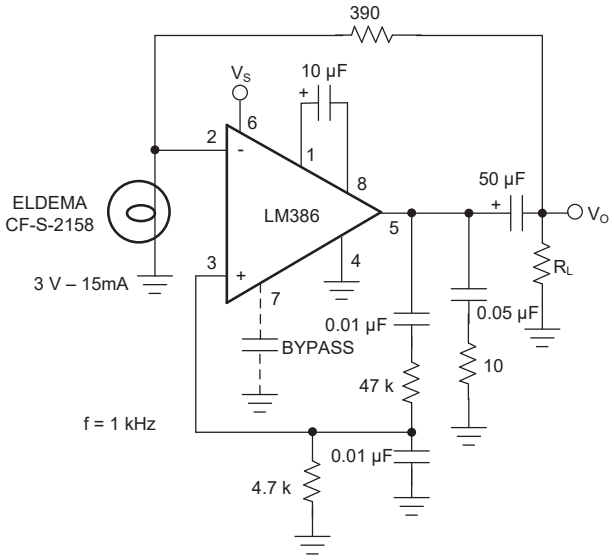

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Figure 16. Low Distortion Power Wienbridge Oscillator

9.2.4.1 Design Requirements

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.4.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the *Detailed Design Procedure* section.

9.2.4.3 Application Curve

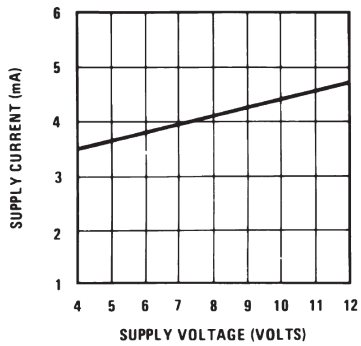

Figure 17. Supply Current vs Supply Voltage

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9.2.5 LM386 with Bass Boost

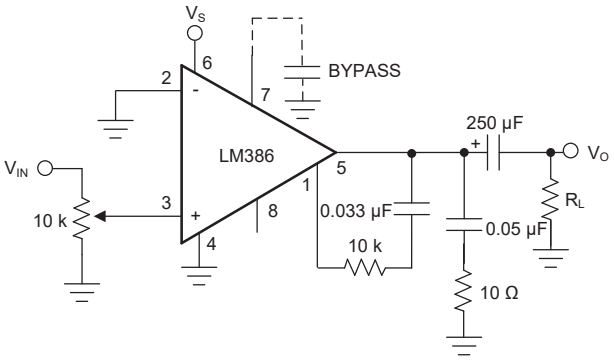

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Figure 18. LM386 with Bass Boost

9.2.5.1 Design Requirements

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.5.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the *Detailed Design Procedure* section.

9.2.5.3 Application Curve

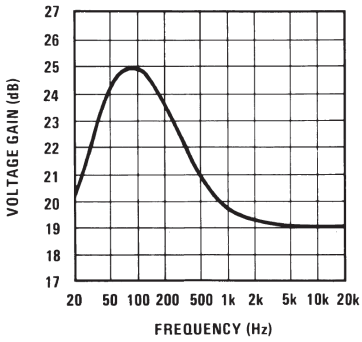

Figure 19. Voltage Gain vs Frequency

9.2.6 Square Wave Oscillator

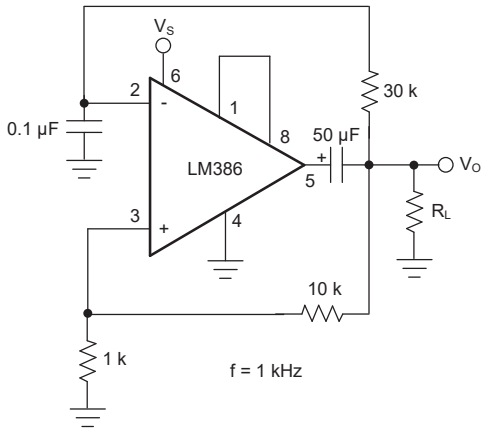

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Figure 20. Square Wave Oscillator

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.6.1 Detailed Design Procedure

The Detailed Design Procedure can be found in the *Detailed Design Procedure* section.

9.2.6.2 Application Curve

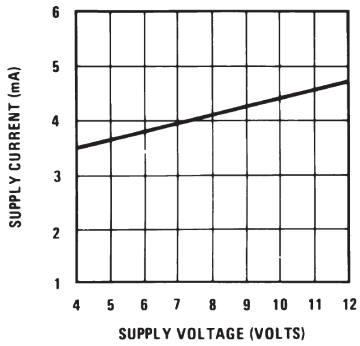

Figure 21. Supply Current vs Supply Voltage

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9.2.7 AM Radio Power Amplifier

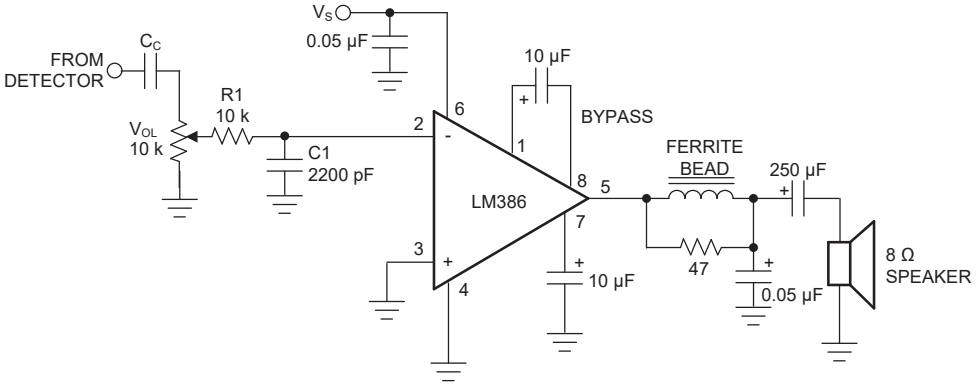

Figure 22. AM Radio Power Amplifier

9.2.7.1 Design Requirements

Table 7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.7.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the *Detailed Design Procedure* section.

9.2.7.3 Application Curve

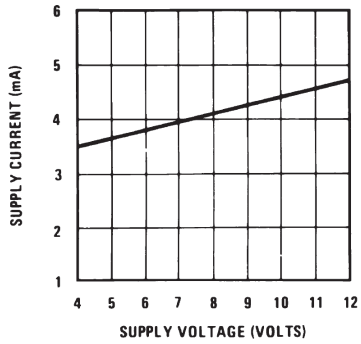

Figure 23. Supply Current vs Supply Voltage

10 Power Supply Recommendations

The LM386 is specified for operation up to 12 V or 18 V. The power supply should be well regulated and the voltage must be within the specified values. It is recommended to place a capacitor to GND close to the LM386 power supply pin.

11 Layout

11.1 Layout Guidelines

Place all required components as close as possible to the device. Use short traces for the output to the speaker connection. Route the analog traces far from the digital signal traces and avoid crossing them.

11.2 Layout Examples

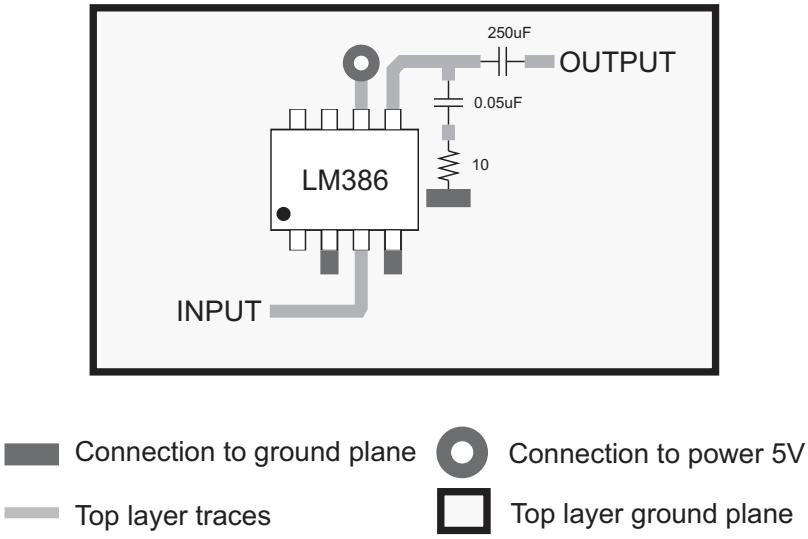

Figure 24. Layout Example for Minimum Parts Gain = 20 dB on PDIP package

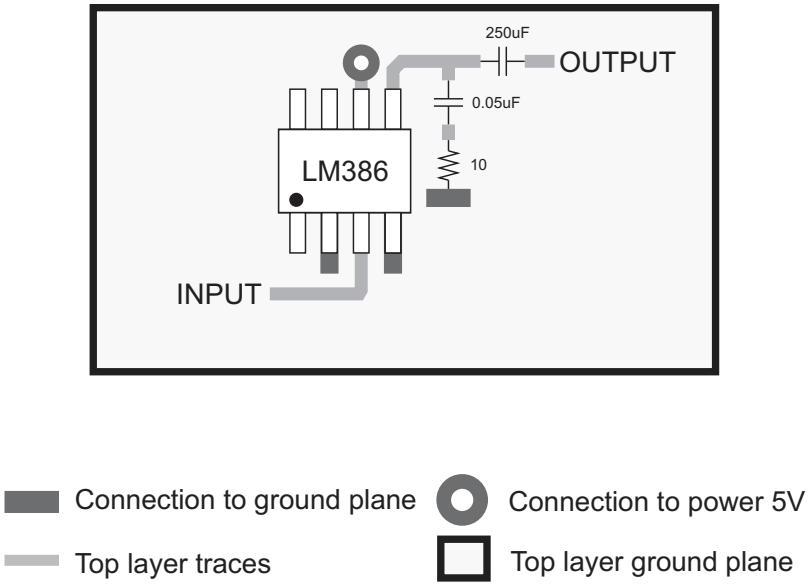

Figure 25. Layout Example for Minimum Parts Gain = 20 dB on SOIC package

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Layout Examples (continued)

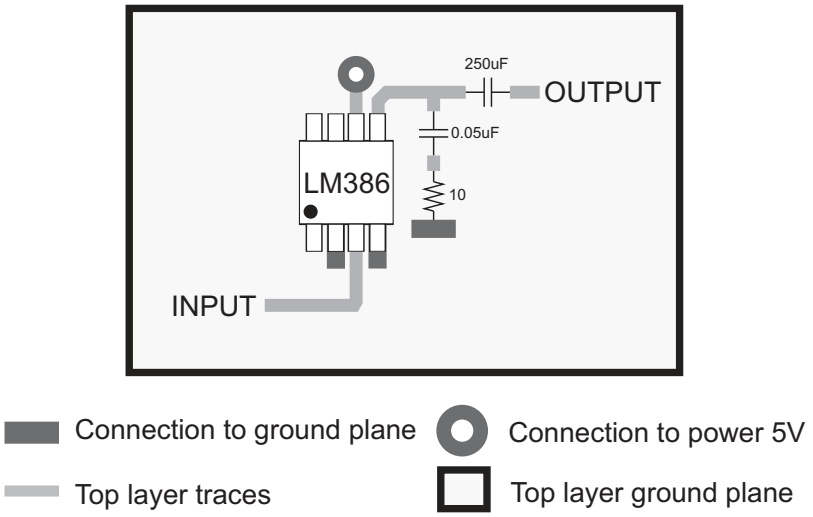

Figure 26. Layout Example for Minimum Parts Gain = 20 dB on VSSOP package

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.2 Documentation Support

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 8. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM386M-1	Click here	Click here	Click here	Click here	Click here
LM386MX-1	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM386M-1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	LM386 M-1	Samples
LM386MMX-1/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	Z86	Samples
LM386MX-1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	LM386 M-1	Samples
LM386N-1/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI | SN	Level-1-NA-UNLIM	0 to 70	LM 386N-1	Samples
LM386N-3/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 70	LM 386N-3	Samples
LM386N-4/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI | SN	Level-1-NA-UNLIM	0 to 70	LM 386N-4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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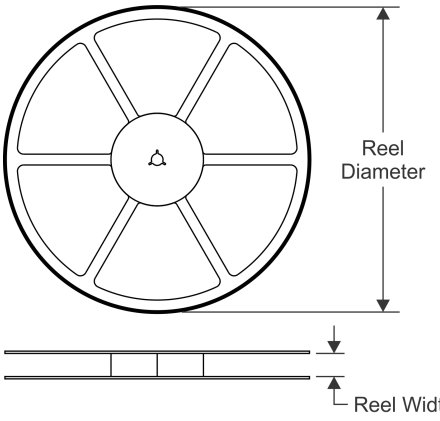
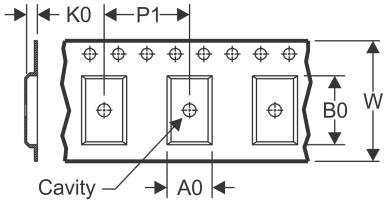
TAPE AND REEL INFORMATION

REEL DIMENSIONS

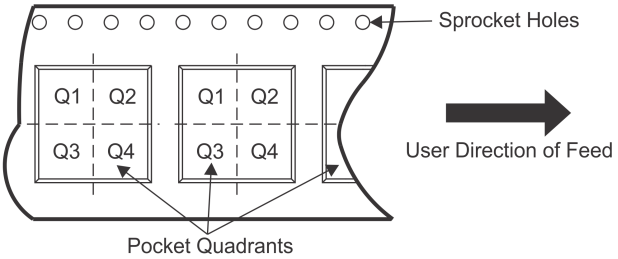


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

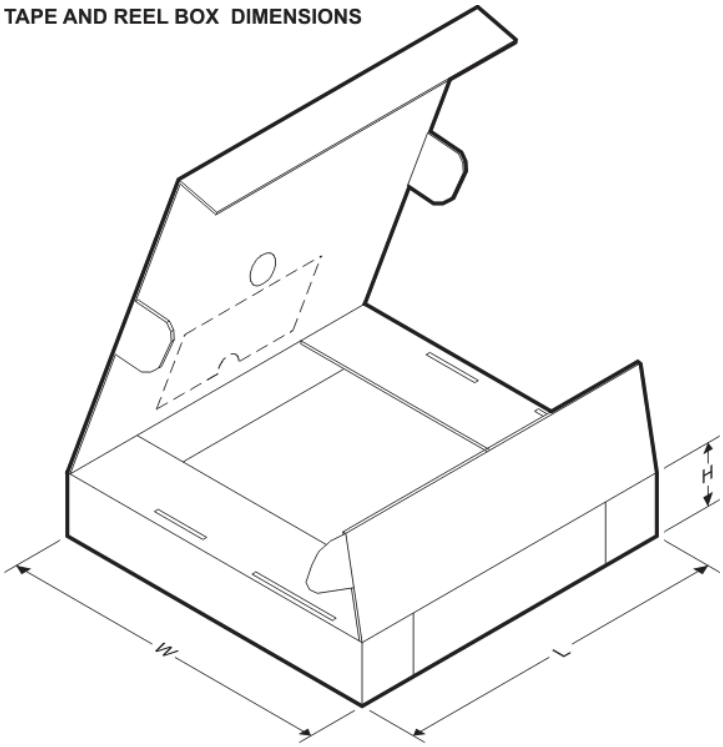
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

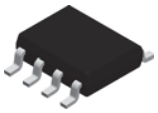
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM386MMX-1/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM386MX-1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM386MMX-1/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM386MX-1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

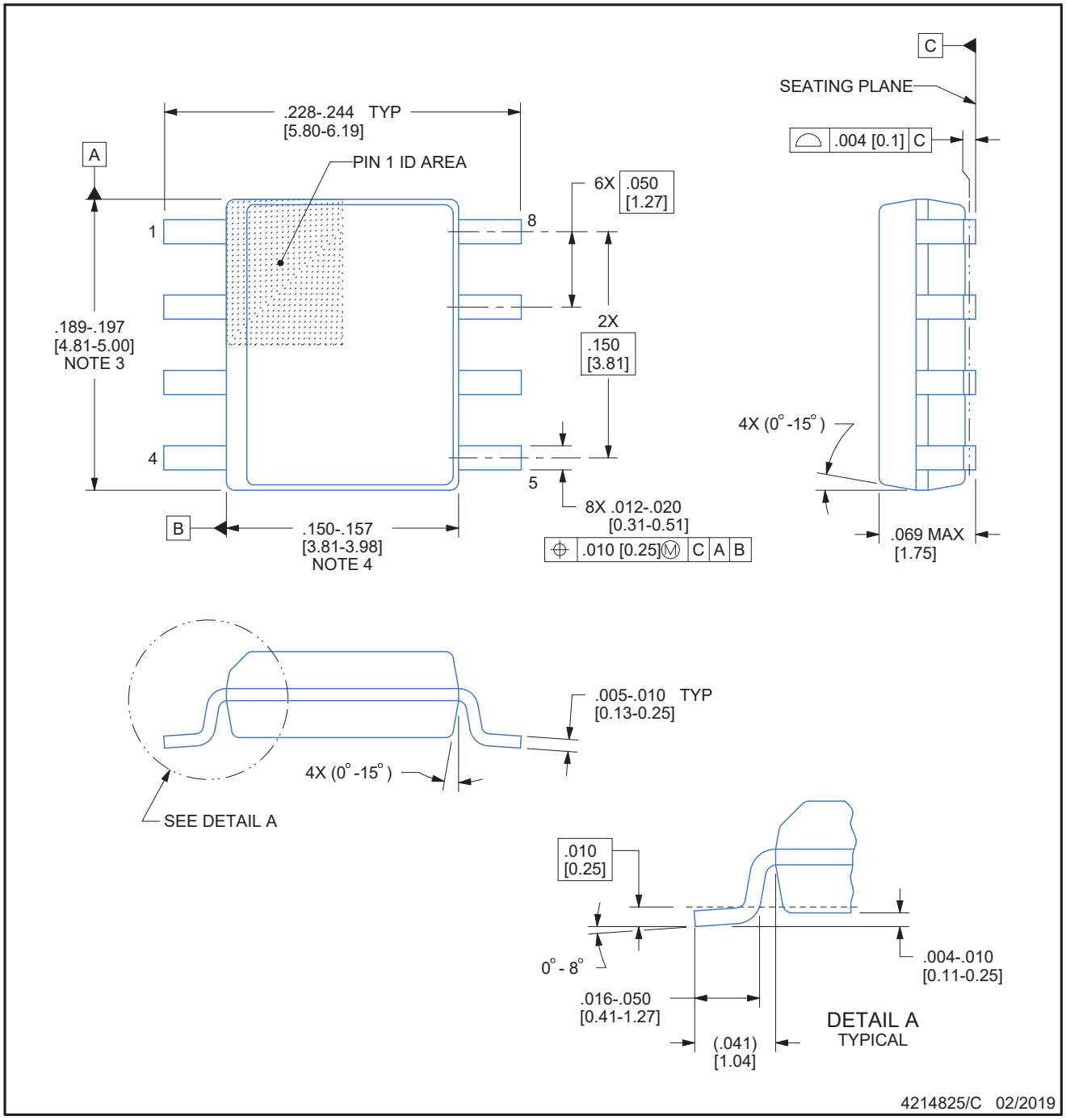


PACKAGE OUTLINE

D0008A

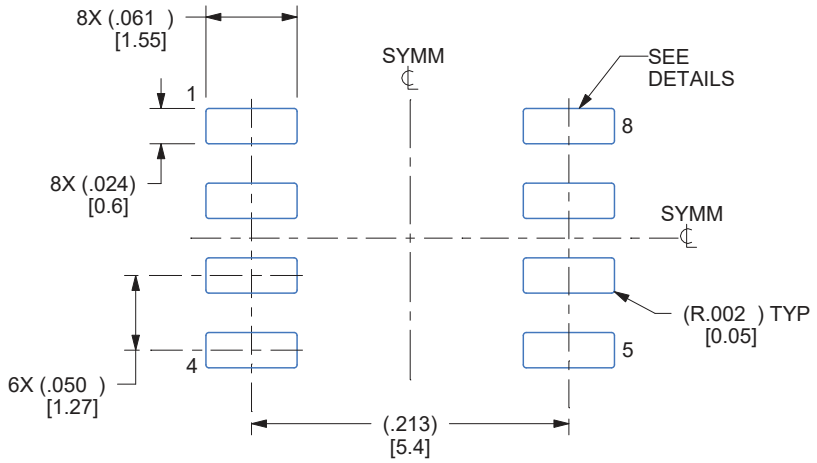
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

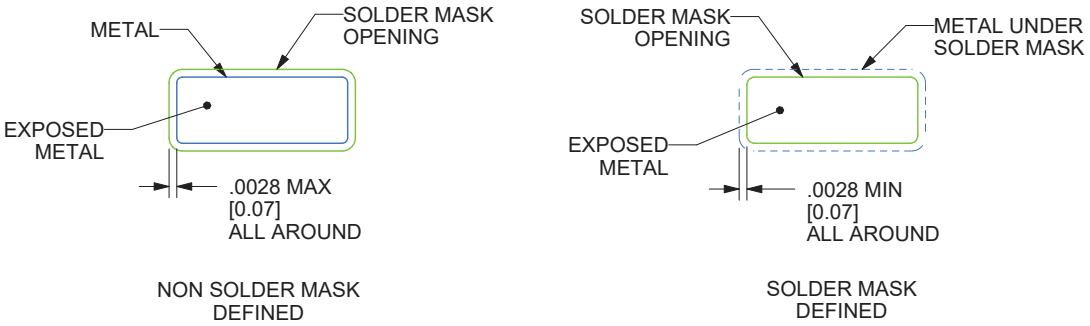


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

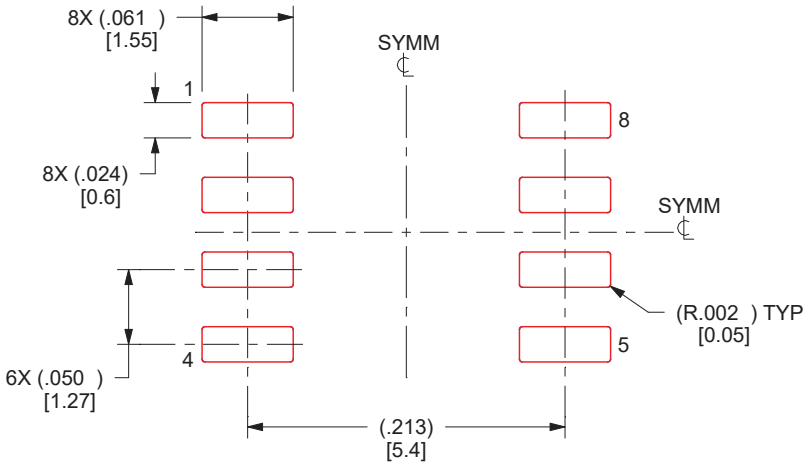


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



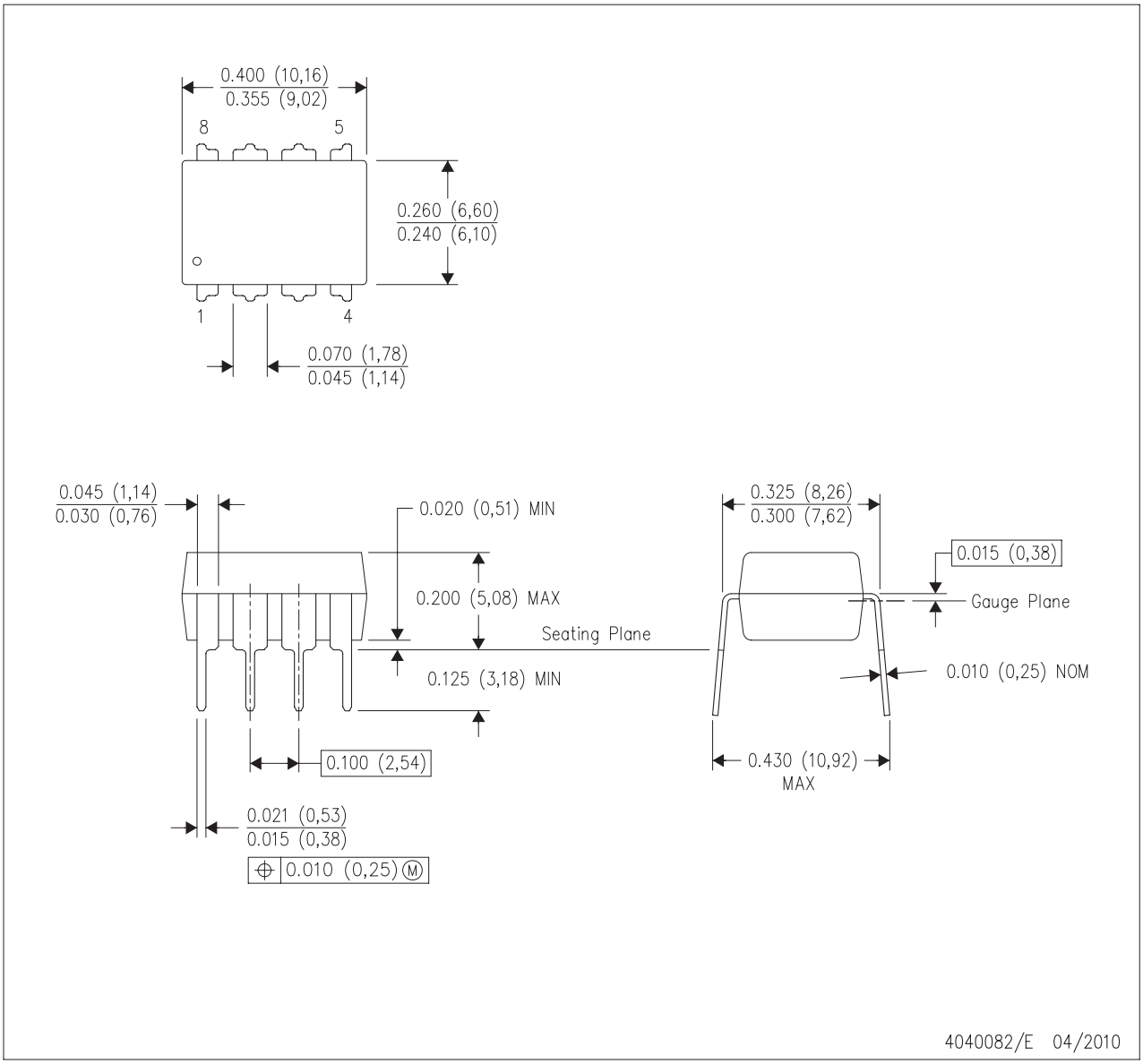
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

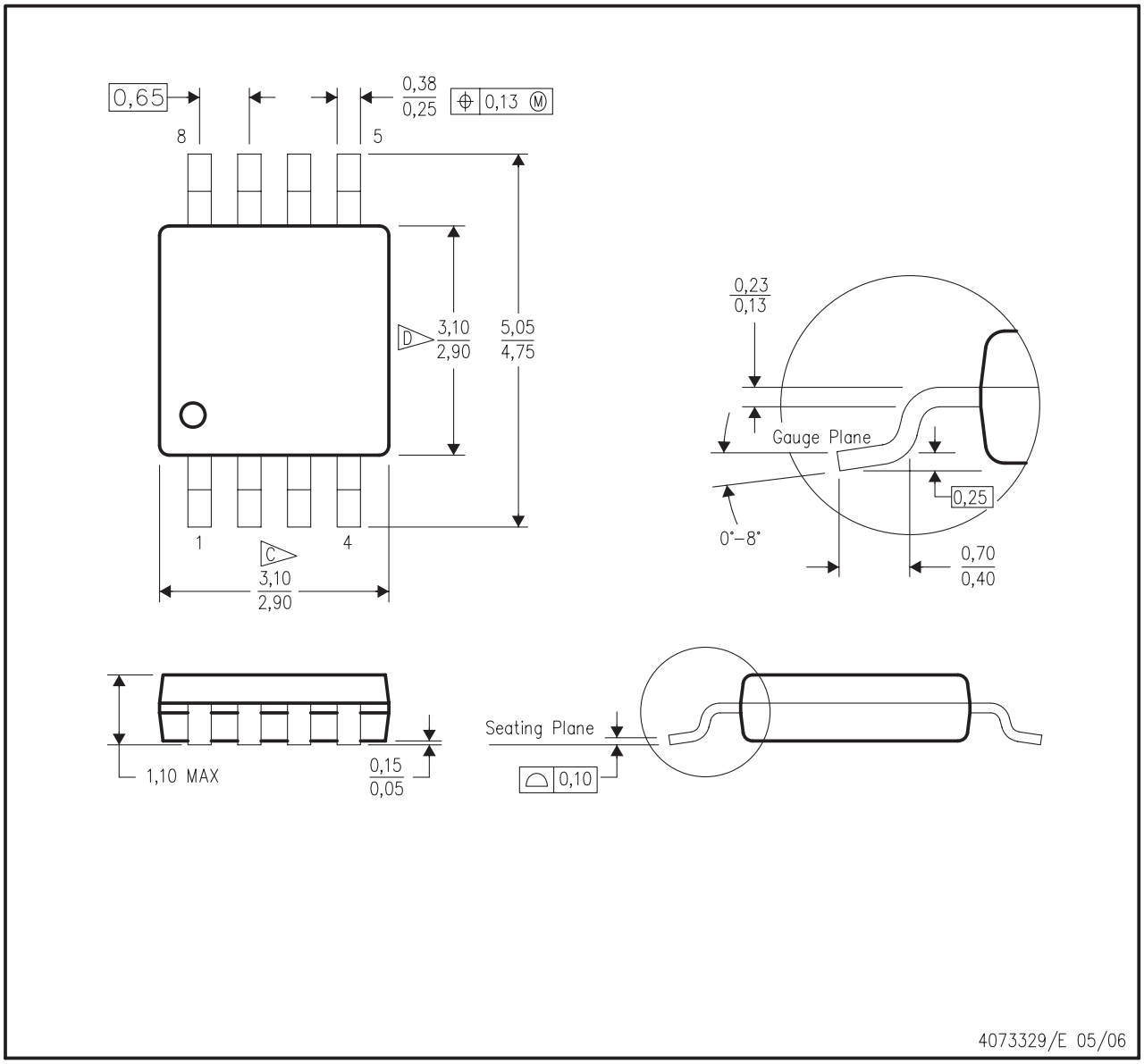
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



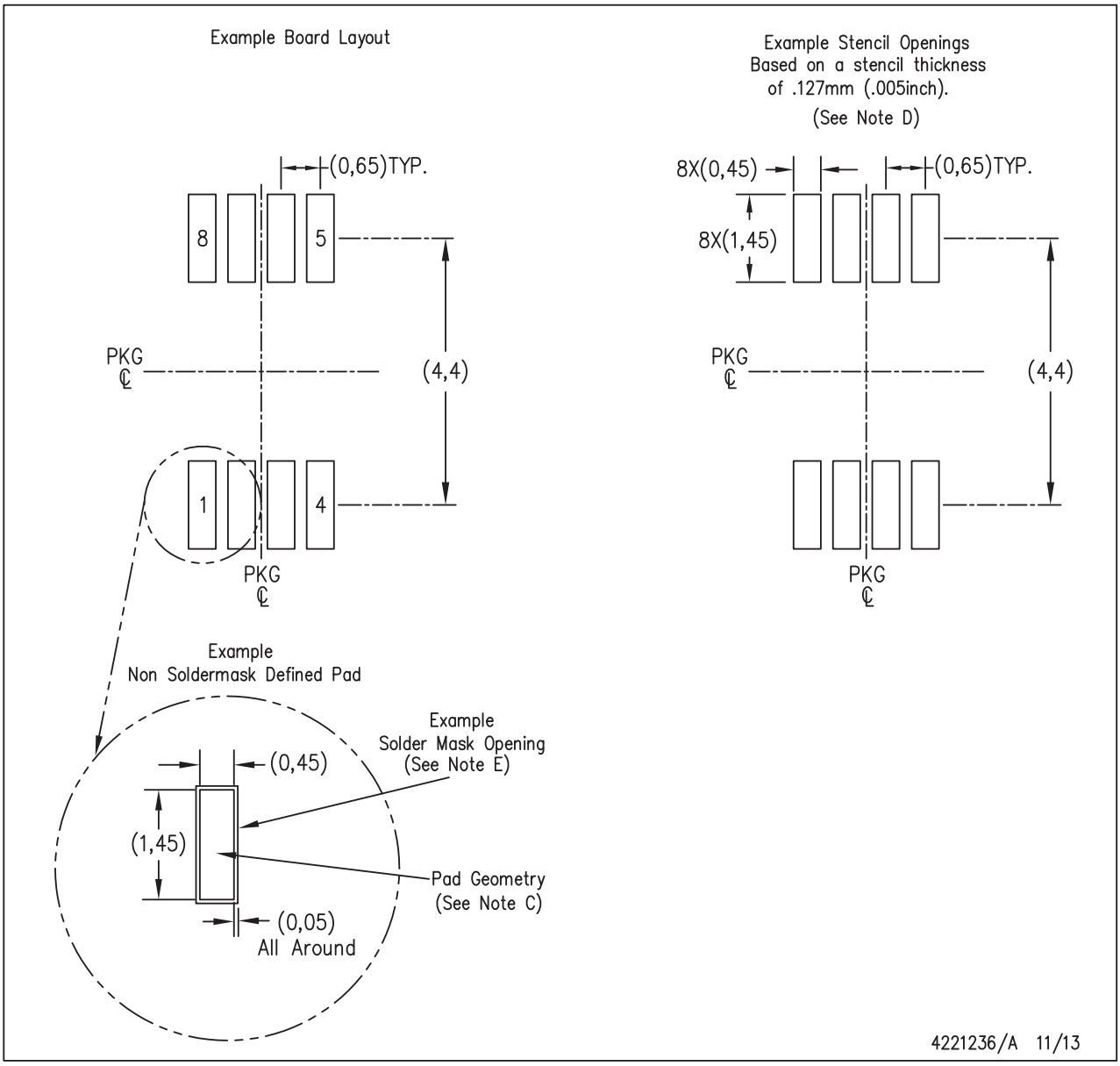
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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